MODELS IN HARDWARE TESTING

FORUM IN HONOR OF CHRISTIAN LANDRAULT

THURSDAY MAY 28, 2009 — SEVILLA, SPAIN

Physical Fault Models and Fault Tolerance

Yves Crouzet and Jean Arlat

{yves.crouzet, jean.arlat}@laas.fr

Université de Toulouse

LAAS-CNRS

Outline

- Fault Models and Off-line/On-line Testing

  —> Yves

- Fault Models and Fault Tolerance Testing

  —> Jean

Fault Models and Off-line/On-line Testing

- Historical Presentation based on Seminal Work Carried out at LAAS-CNRS (1975-1980)
- Study Directed by Christian in the Frame of an Industrial Research Contract and of My PhD
- First Work By Christian Devoted To Hardware Testing
- *Fac Simile* "Vintage" Slides from Christian and myself… ☺

Y. Crouzet, C. Landrault Design of Self-Checking MOS-LSI Circuits - Application to a Four-Bit Microprocessor
FTCS-9, Madison, Wisconsin (USA), June 1979, pp. 189-192

J. Galiay, Y. Crouzet, M. Vergniault Physical vs. Logical Faults Models in MOS-LSI Circuits - Impact on Their Testability
FTCS-9, Madison, Wisconsin (USA), June 1979, pp. 195-202.

Y. Crouzet Fault Models in Single Channel MOS Technology
1st European Workshop on Design for Testability, Sept. 29 - Oct. 1 1982, Toulon, France.

FAULT MODELS

IN MONOCHANNEL MOS TECHNOLOGY

→ FIRST PART OF A RESEARCH
AND DEVELOPMENT PROJECT

L.A.A.S. + E.F.C.I.S.

PROJECT SPONSORED BY D.R.E.T.

AIM OF THIS PROJECT

DESIGN OF LSI CIRCUITS WITH ENHANCED TESTABILITY

- EASILY TESTABLES CIRCUITS
- SELF-TESTING CIRCUITS

REALIZATION OF EASILY-TESTABLE
OR SELF-TESTING CIRCUITS

→ KNOWLEDGE OF THE FAULT MODELS IS CRUCIAL

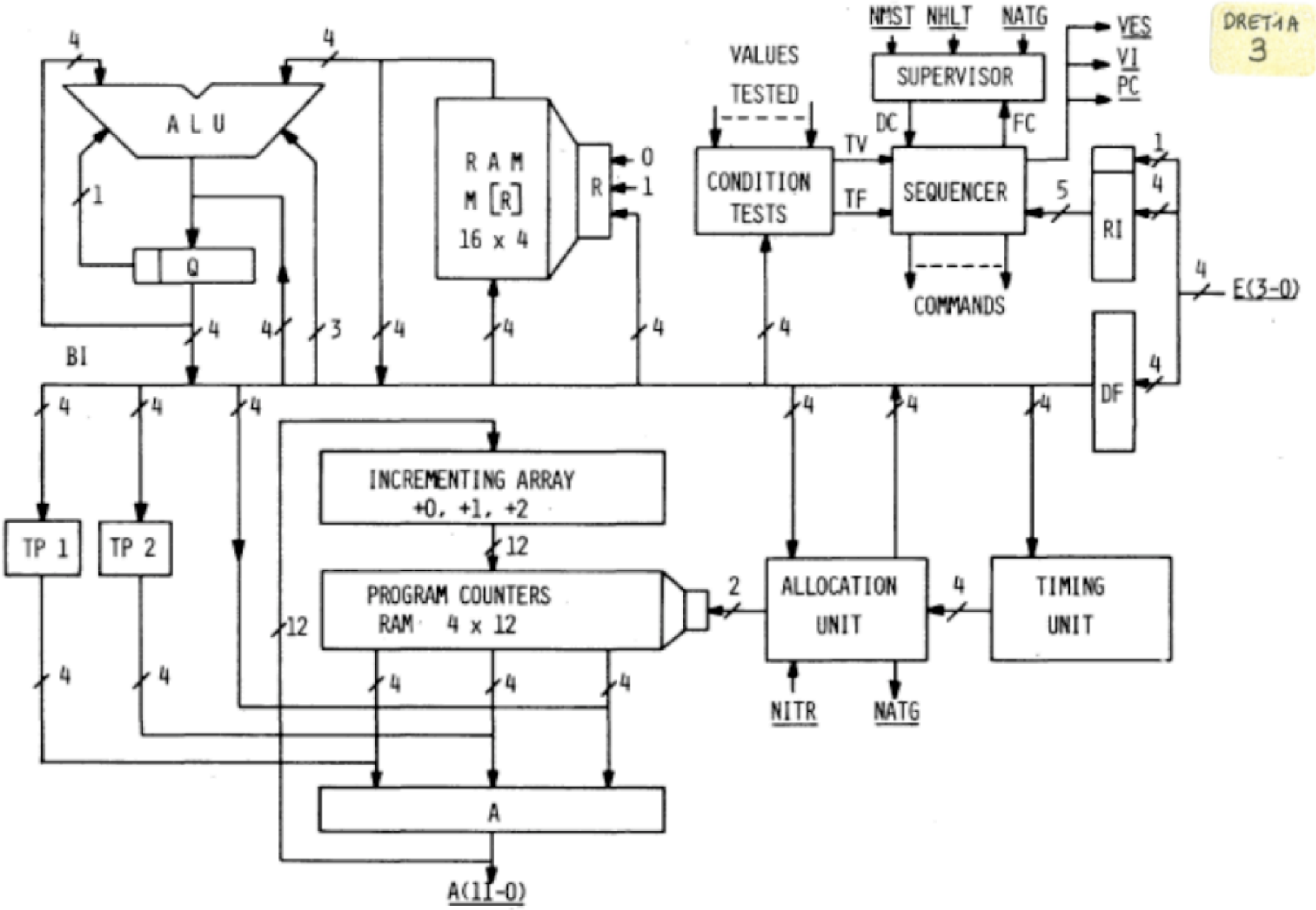
STUCK-AT : THE MOST OFTEN-CONSIDERED FAULT MODEL

→ SATISFACTORY FOR SMALL-SCALE INTEGRATION

→ QUESTIONABLE VALIDITY FOR LARGE-SCALE INTEGRATION

TO REPLY TO SUCH A QUESTION

→ CHARACTERIZATION OF LSI FAILURE MODES ON A SET OF FAILED CIRCUITS AT THE MANUFACTURE PHASE


DRET1A
3
NMST
NHLT
NATG
VES
VI
PC
VALUES
TESTED
SUPERVISOR
DC
FC
TV
TF
CONDITION
TESTS
SEQUENCER
COMMANDS
RI
E(3-0)
A L U
Q
R A M
M [R]
16 x 4
R
0
1
BI
DF
INCREMENTING ARRAY
+0, +1, +2
TP 1
TP 2
PROGRAM COUNTERS
RAM 4 x 12
ALLOCATION
UNIT
TIMING
UNIT
NITR
NATG
A
A(11-0)

- CHARACTERIZATION OF THE FAILURES

  .AUTOMATIC PRELOCALIZING SEQUENCE : START-SMALL APPROACH

    .DIVIDED INTO SEVERAL SUBSEQUENCES

    .HIERARCHICAL SUCCESSION OF THE SUBSEQUENCES

  .DIRECT INSPECTION ON THE CHIP

    .PARAMETRIC MEASURING

    .SCHMOO PLOT

    .VISUAL INSPECTION

    .POTENTIAL CARTOGRAPHY

    .PUNCTUAL ANALYSIS

RESULTS OF PRACTICAL ANALYSIS

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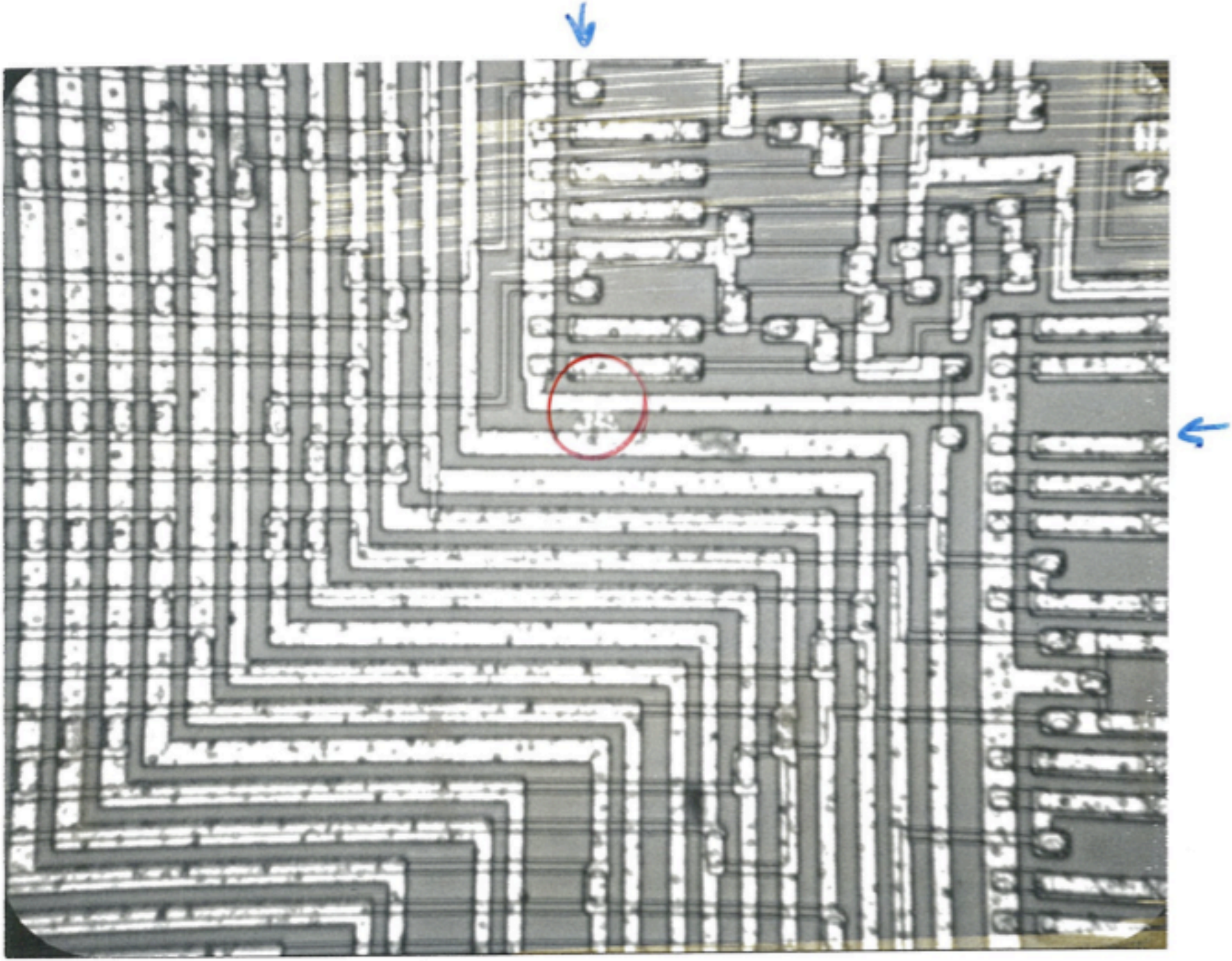
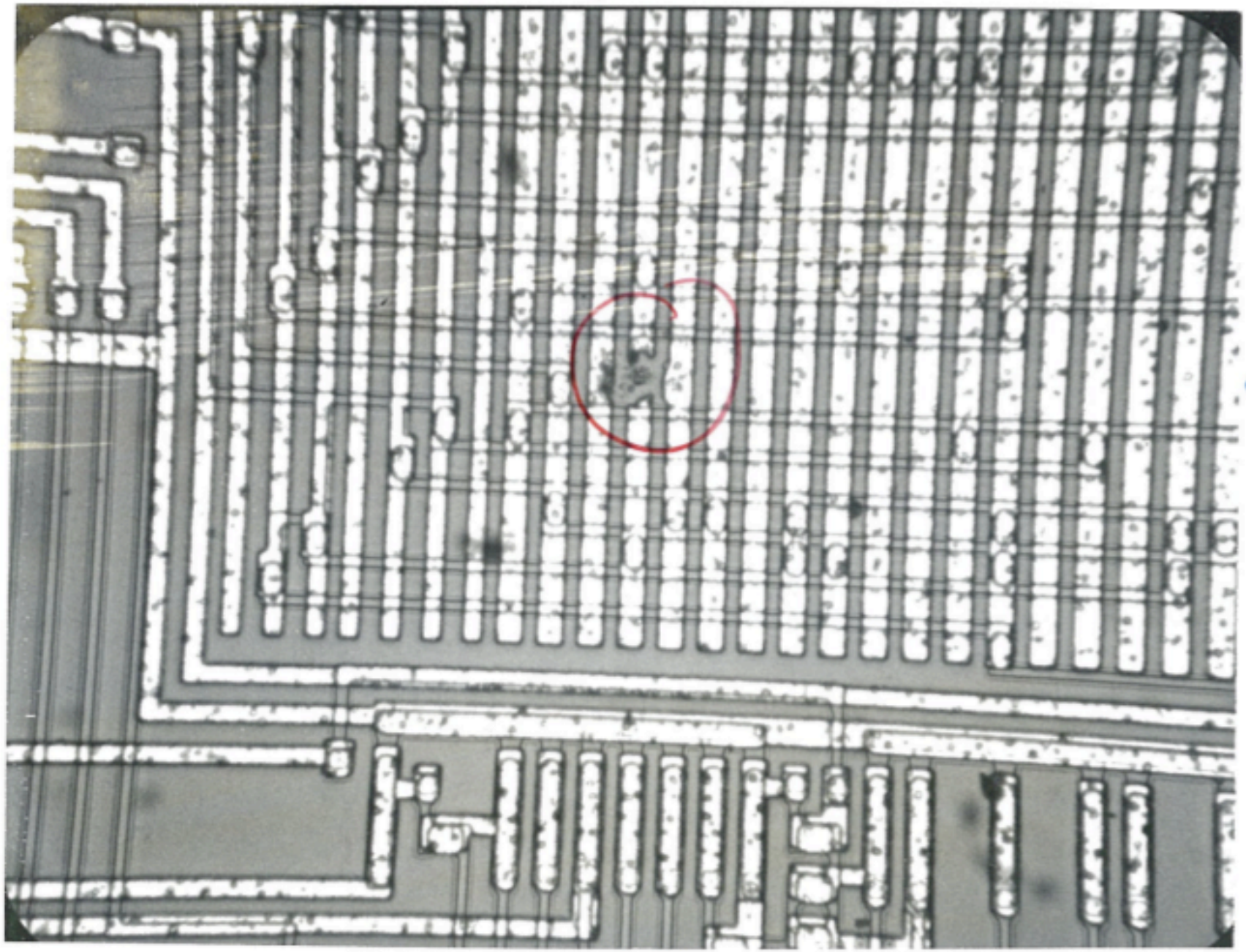
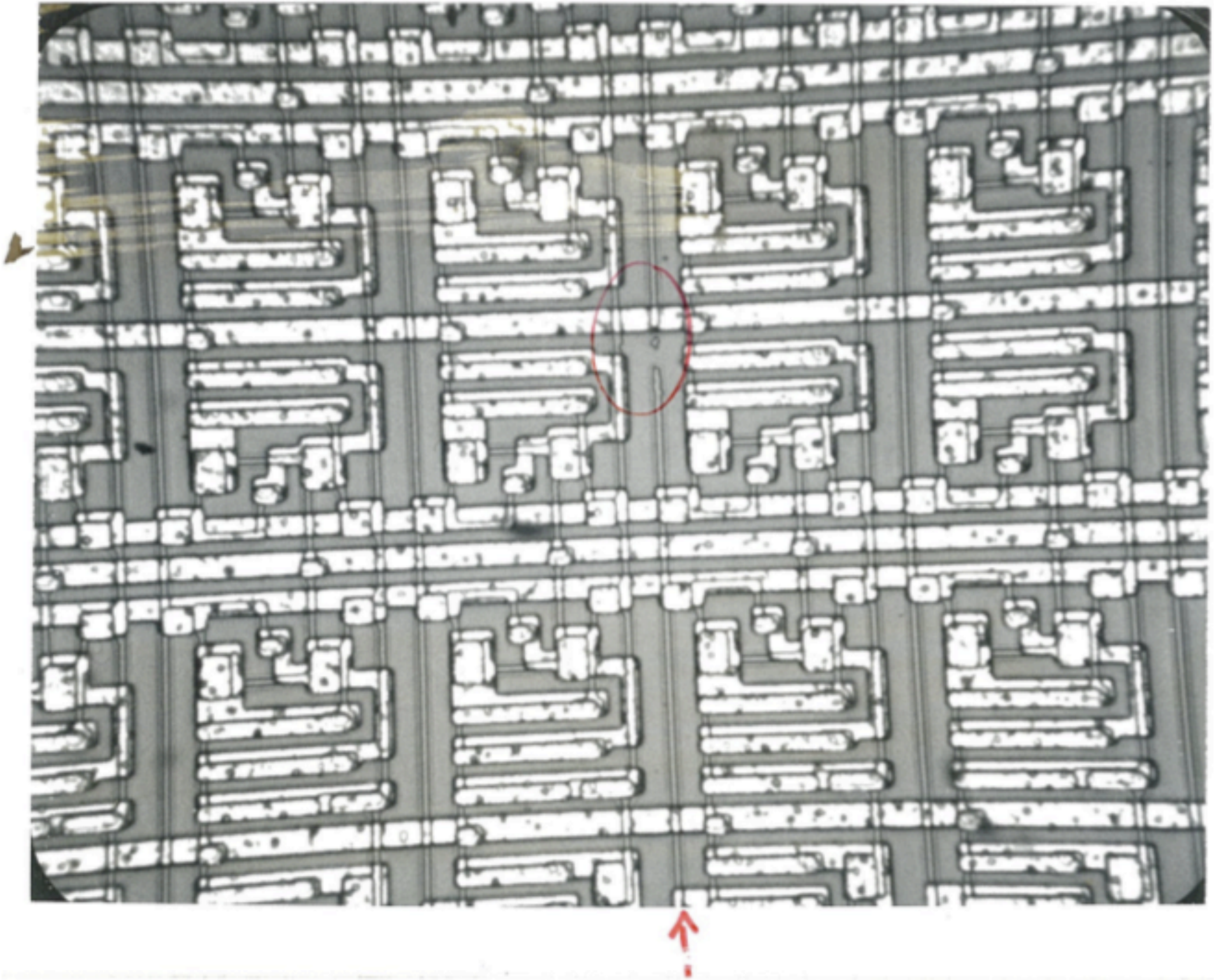
- FAILURES UNIFORMLY DISTRIBUTED ON THE WHOLE CHIP

SHORT BETWEEN METALLIZATIONS	39 %
CUT OF A METALLIZATION	14 %
SHORT BETWEEN DIFFUSIONS	14 %
CUT OF A DIFFUSION	6 %
SHORT BETWEEN METALLIZATION AND SUBSTRATE	2 %
INOBSERVABLE	10 %
INSIGNIFICANT	15 %

REMARK : NO SHORT BETWEEN METALLIZATION AND DIFFUSION







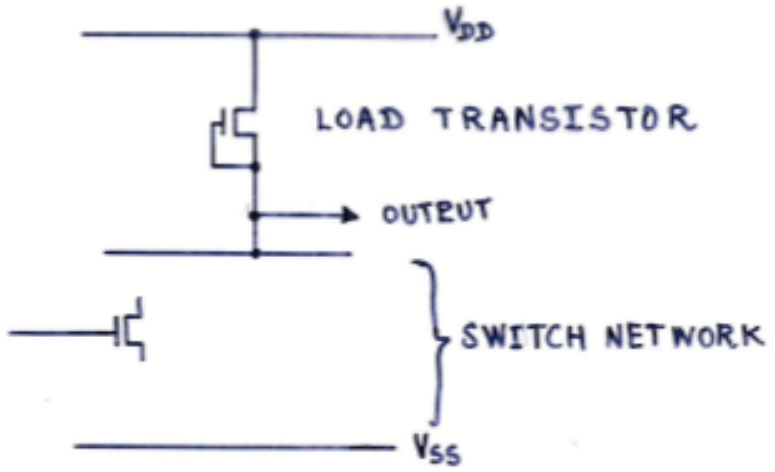
DEFINITIONS

FAILURE : PHYSICAL DEFECT (SHORT, OPEN,
THRESHOLD VOLTAGE DRIFT

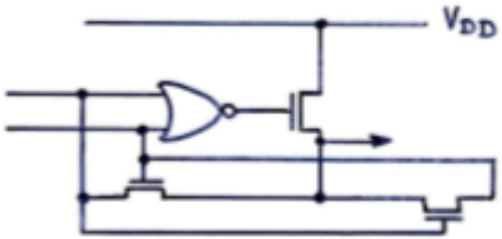
FAULT : LOGICAL MODEL OF A FAILURE

STUCK-AT : MODEL MOST OFTEN USED

ERROR : DEVIATION OF THE OUTPUT WITH
REFERENCE TO THE CORRECT OPERATION



GATE WITH CLASSICAL STRUCTURE



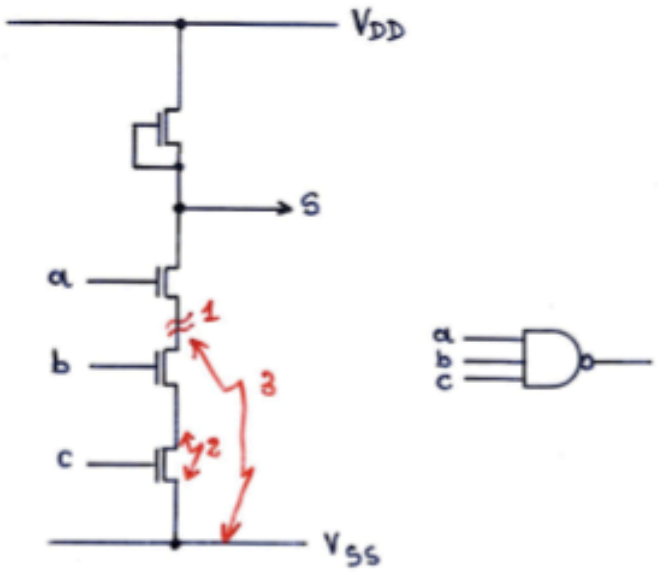
GATE WITH NON-CLASSICAL STRUCTURE

GATES WITH CLASSICAL STRUCTURE ⟶ GENERAL RESULTS

TWO CASES ARE CONSIDERED :

- ELEMENTARY GATES (AND, OR STRUCTURE)
- COMPLEX GATES (AND-OR, OR-AND STRUCTURE)

FAILURES IN ONE ELEMENTARY GATE



NAND GATE

FAULT MODELS

OPEN 1 → OUTPUT STUCK-AT 1
ANY INPUT STUCK-AT 0

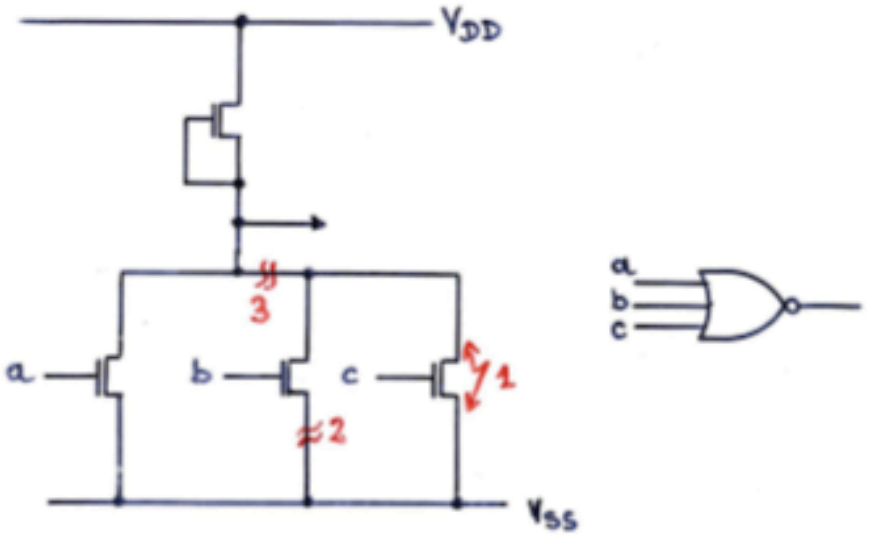
SHORT 2 → INPUT C STUCK-AT 1

SHORT 3 → INPUTS B,C STUCK-AT 1

ERROR MODELS

OPEN → ERROR-AT 1

SHORT → ERROR-AT 0



NOR GATE

FAULT MODELS

SHORT 1 ⟶ OUTPUT STUCK-AT 0
ANY INPUT STUCK-AT 1

OPEN 2 ⟶ INPUT B STUCK-AT 0

OPEN 3 ⟶ INPUTS B,C STUCK-AT 0

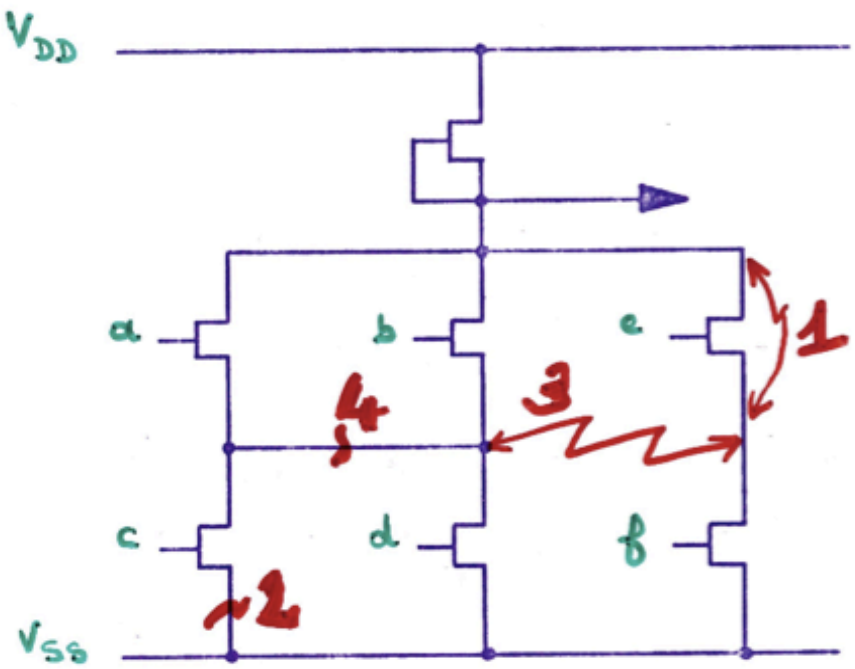
ERROR MODELS

OPEN ⟶ ERROR-AT 1

SHORT ⟶ ERROR-AT 0

II. CONSEQUENCES OF FAILURE MODES

1) ALL FAILURES CANNOT BE MODELLED BY STUCK-AT FAULTS



- ALL SHORTS OR CUTS OF ONE TRANSISTOR (1, 2)

→ STUCK AT FAULTS

- SHORTS OR CUTS OF INTERCONNECTIONS BETWEEN TRANSISTORS CANNOT BE MODELLED BY STUCK-AT FAULTS (3,4)

→ MODIFICATION OF THE FUNCTION

2) INADEQUACY OF THE LOGICAL DIAGRAM

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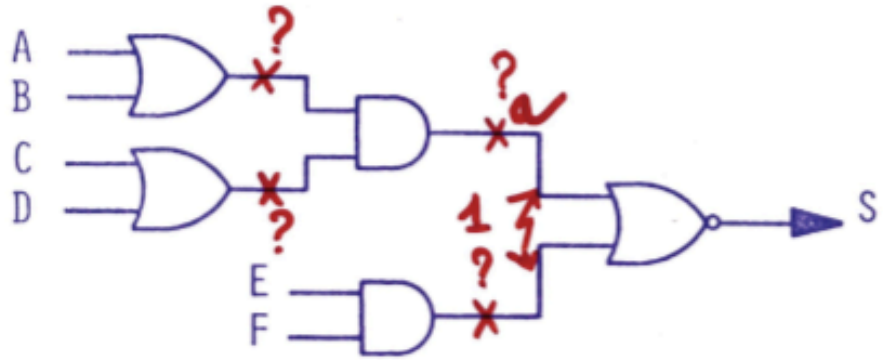
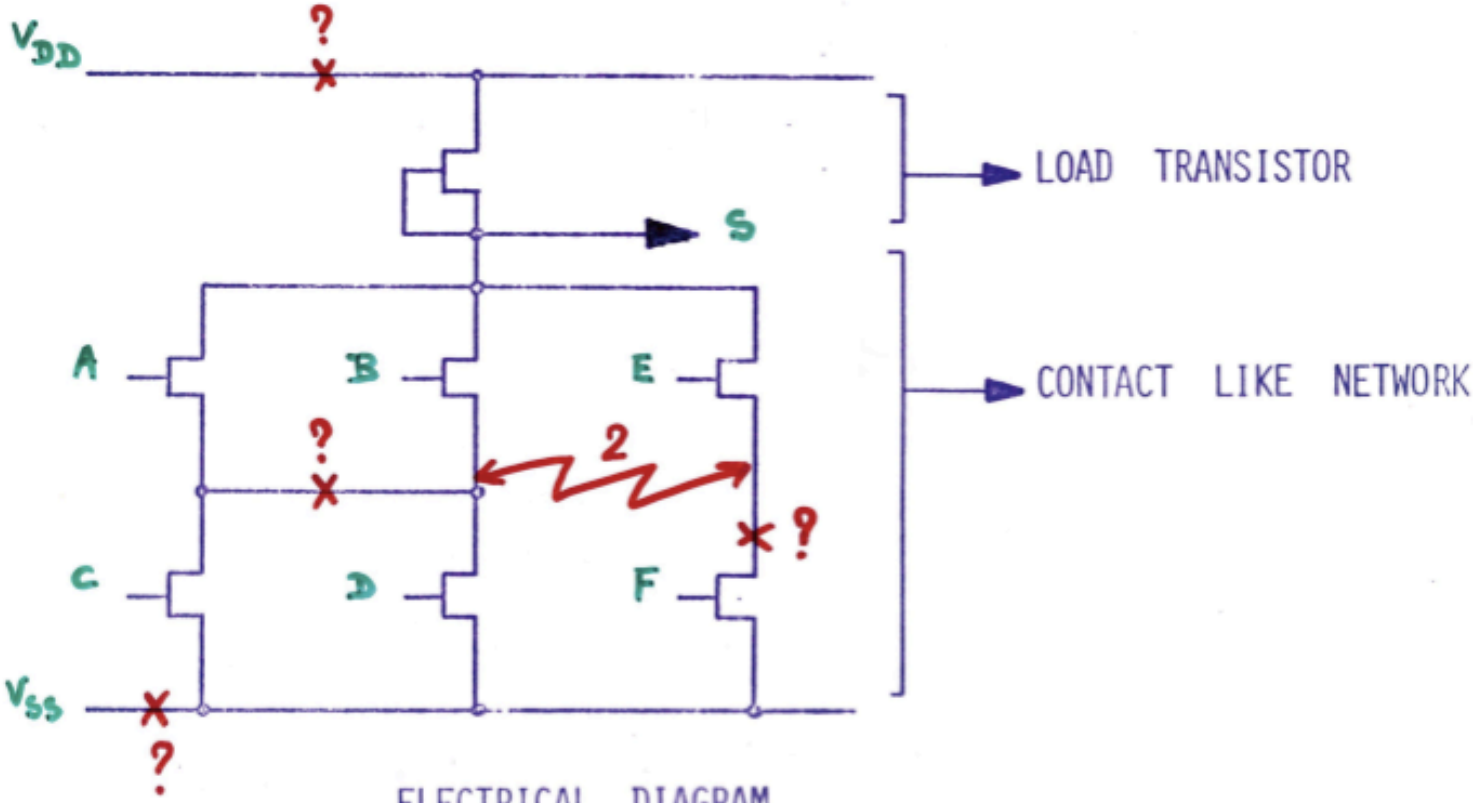
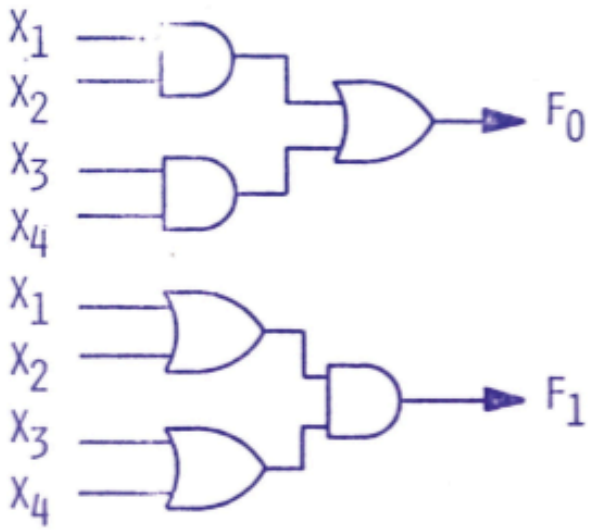


LOGICAL DIAGRAM



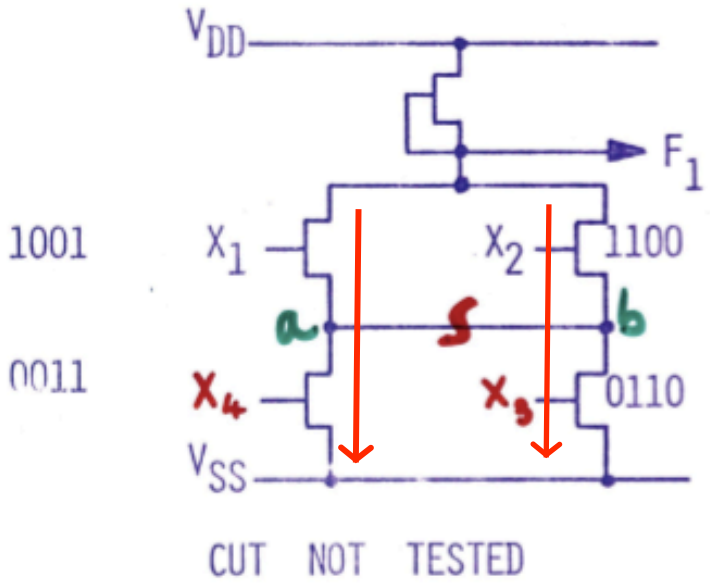
ELECTRICAL DIAGRAM

EXAMPLE : CHECKER 2-OUT-OF-4 CODE (ANDERSON)

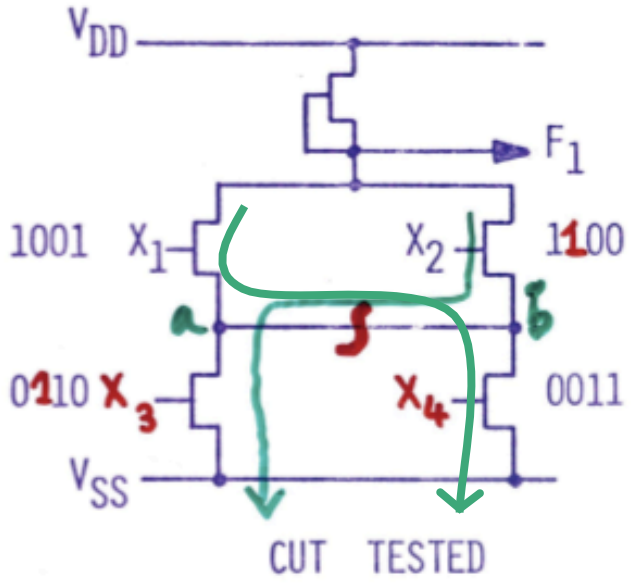


TEST VECTORS (4)

X_1	X_2	X_3	X_4
1	1	0	0
0	1	1	0
0	0	1	1
1	0	0	1



CUT NOT TESTED



CUT TESTED

DEPENDING ON X_3 AND X_4

III. GENERATION OF TEST SEQUENCES

HOW TO APPROACH THE TEST SEQUENCE GENERATION PROBLEM ?

1. DIRECT CONSIDERATION OF ALL SHORTS AND CUTS :

PB : NEED TO KNOW THE ELECTRICAL REPRESENTATION

.CUTS ⟶ FEASIBLE

.SHORTS ⟶ GREAT DIFFICULTIES BECAUSE OF

.VERY NUMEROUS POSSIBILITIES OF SHORTS

.SHORT EFFECT ANALYSIS GENERALLY DIFFICULT

.FOR SOME SHORTS THERE EXISTS NON PRE-ESTABLISHED TEST SEQUENCE

2. PREVENTION OF SOME FAILURE POSSIBILITIES IS A MORE REALISTIC APPROACH : EASILY TESTABLE APPROACH ⟶ LAYOUT RULES

B) LAYOUT RULES AT THE GATE LEVEL

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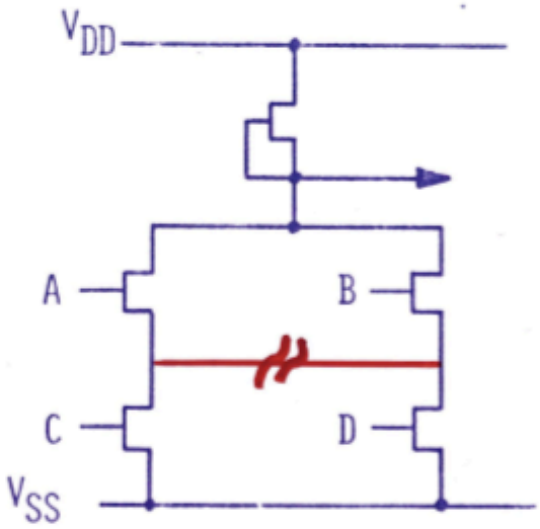
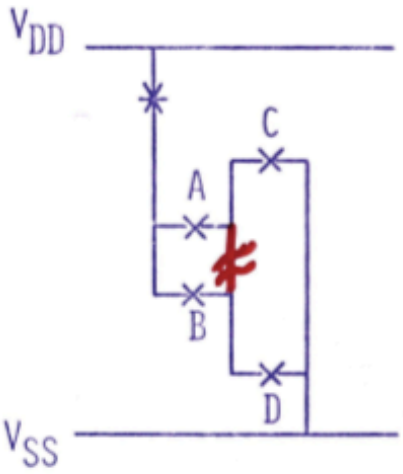
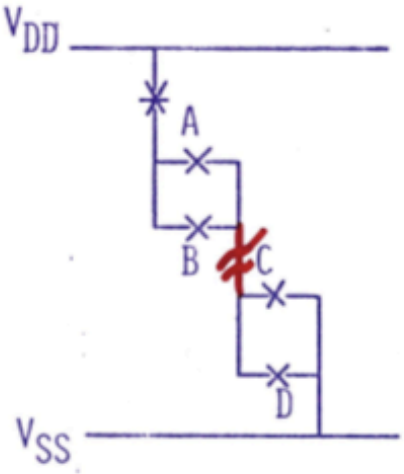






✳ : LOAD TRANSISTOR

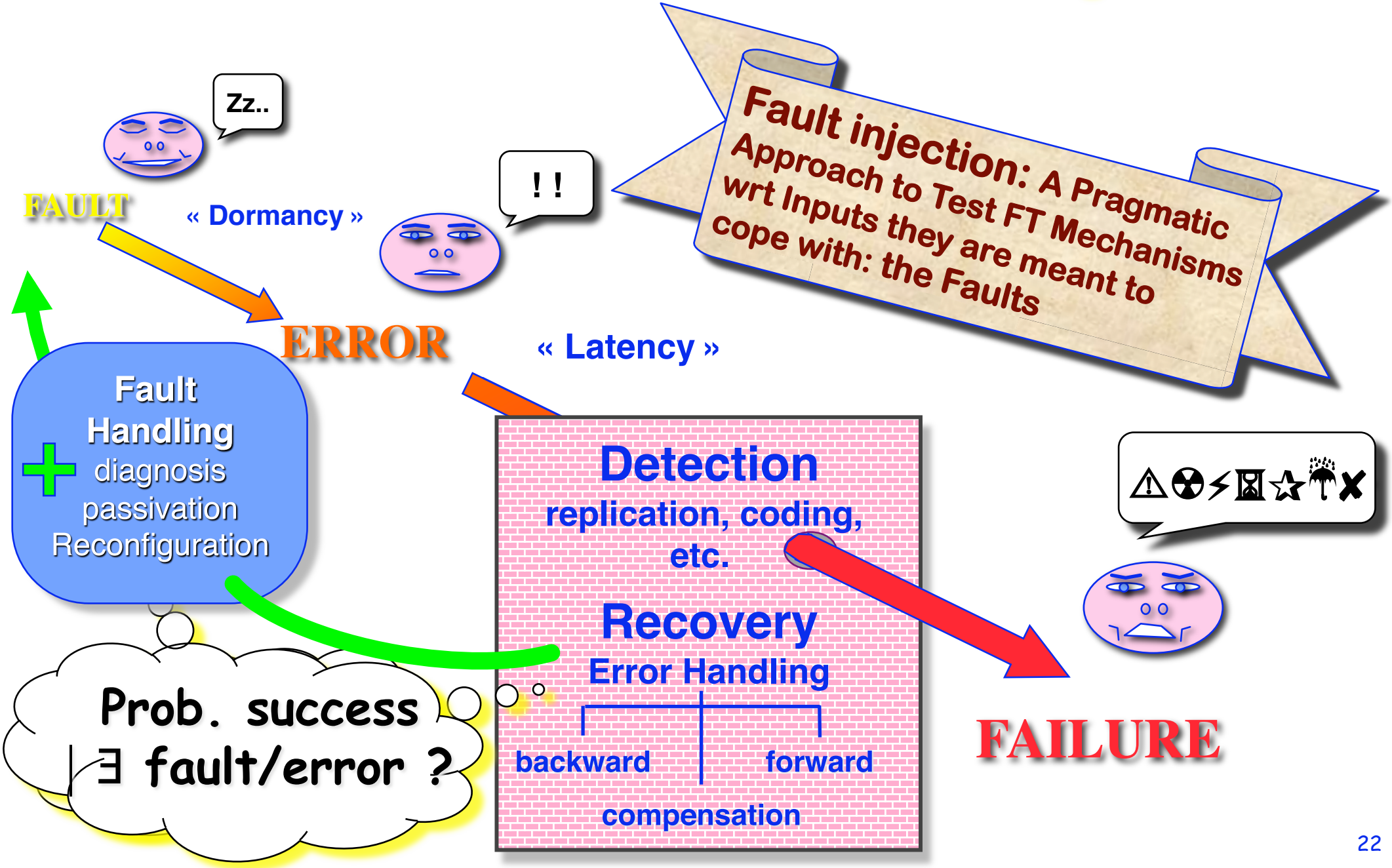
× : COMMAND TRANSISTOR

Fault Models and Fault Tolerance Testing

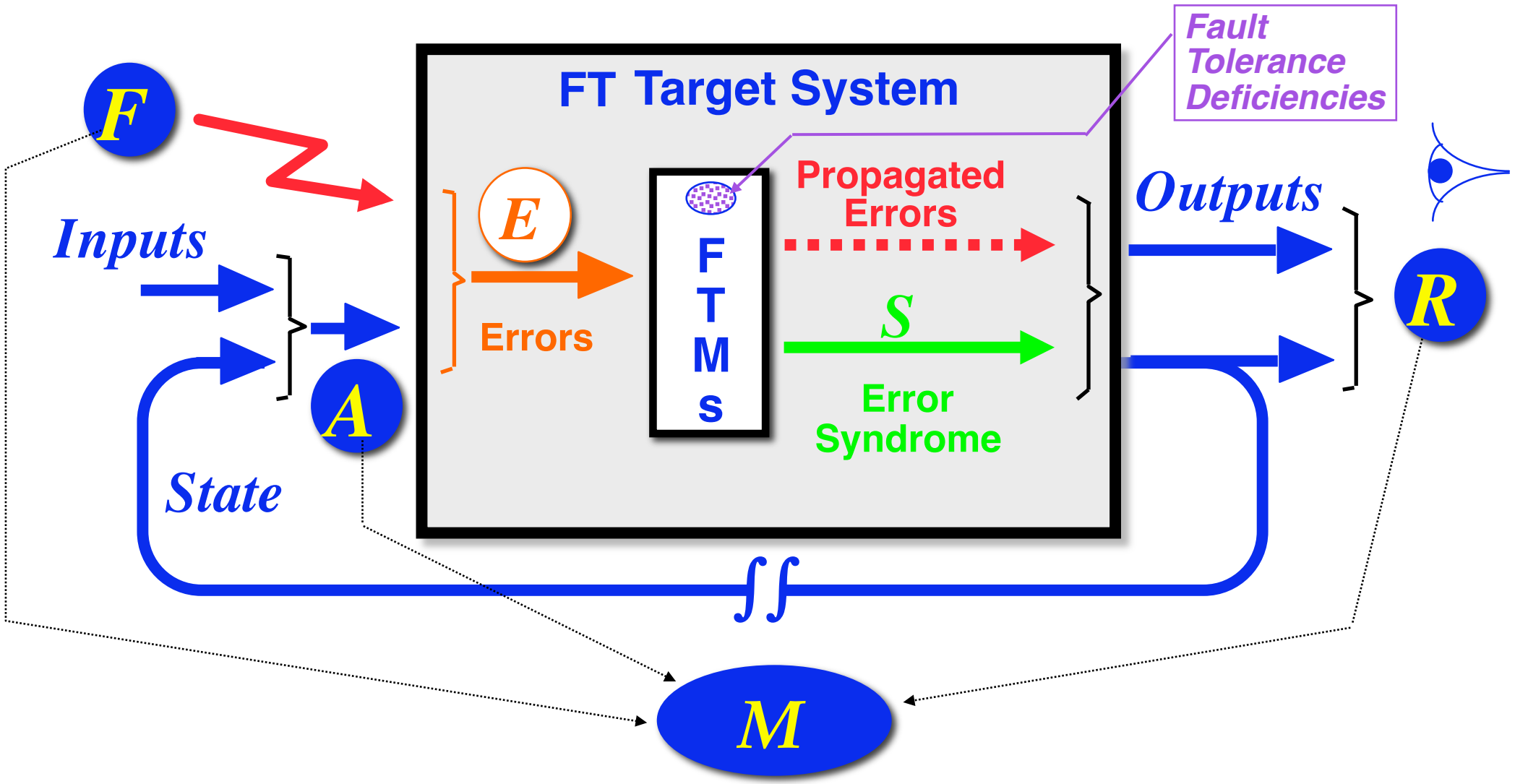
- Dependable Circuits and Systems
  —> Fault-Tolerant Architectures
- Assessment of Fault Tolerance
- Formal Verification, Analytical Evaluation, …

—> Empirical Approach: Fault Injection

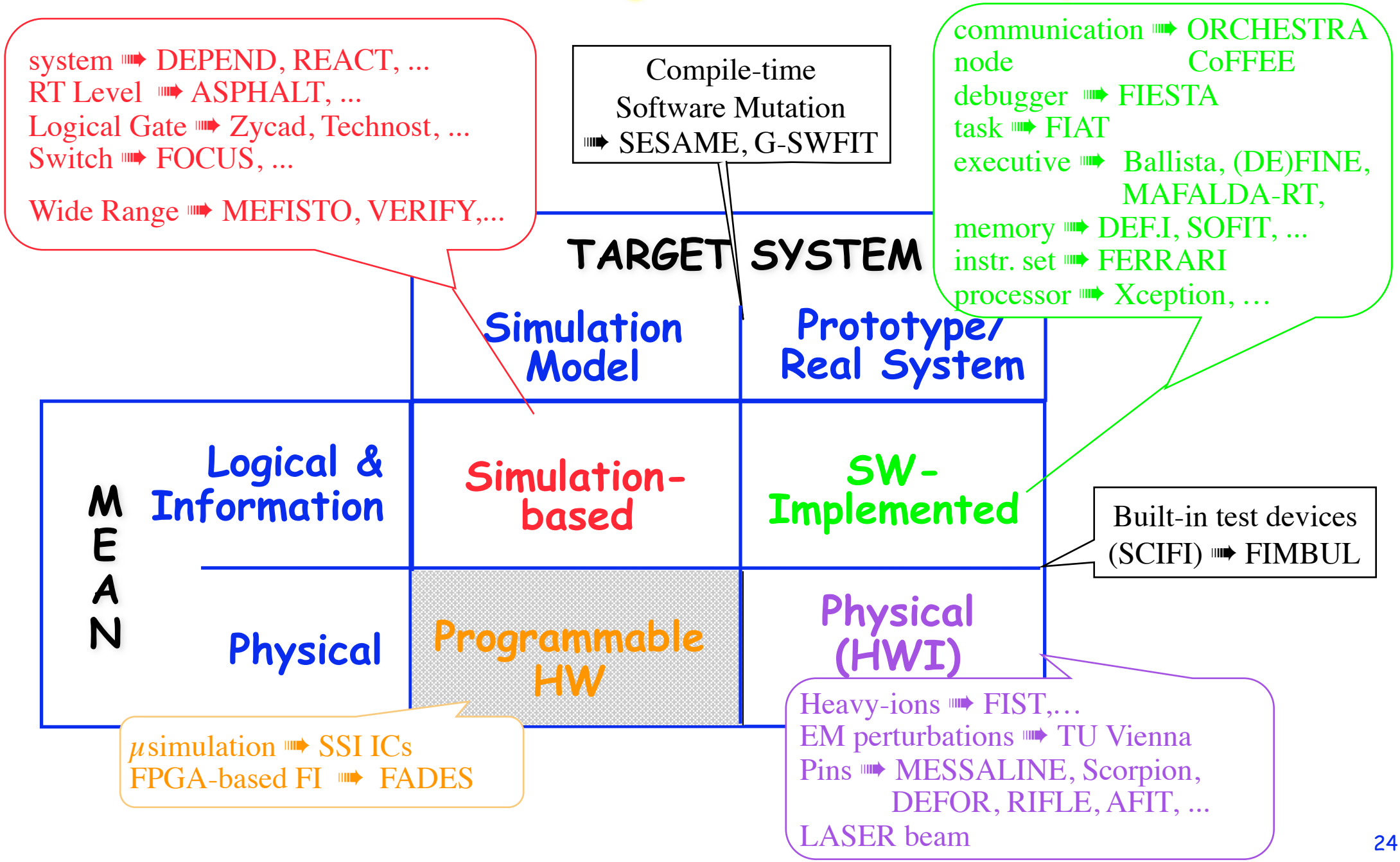
Fault Tolerance … and Coverage



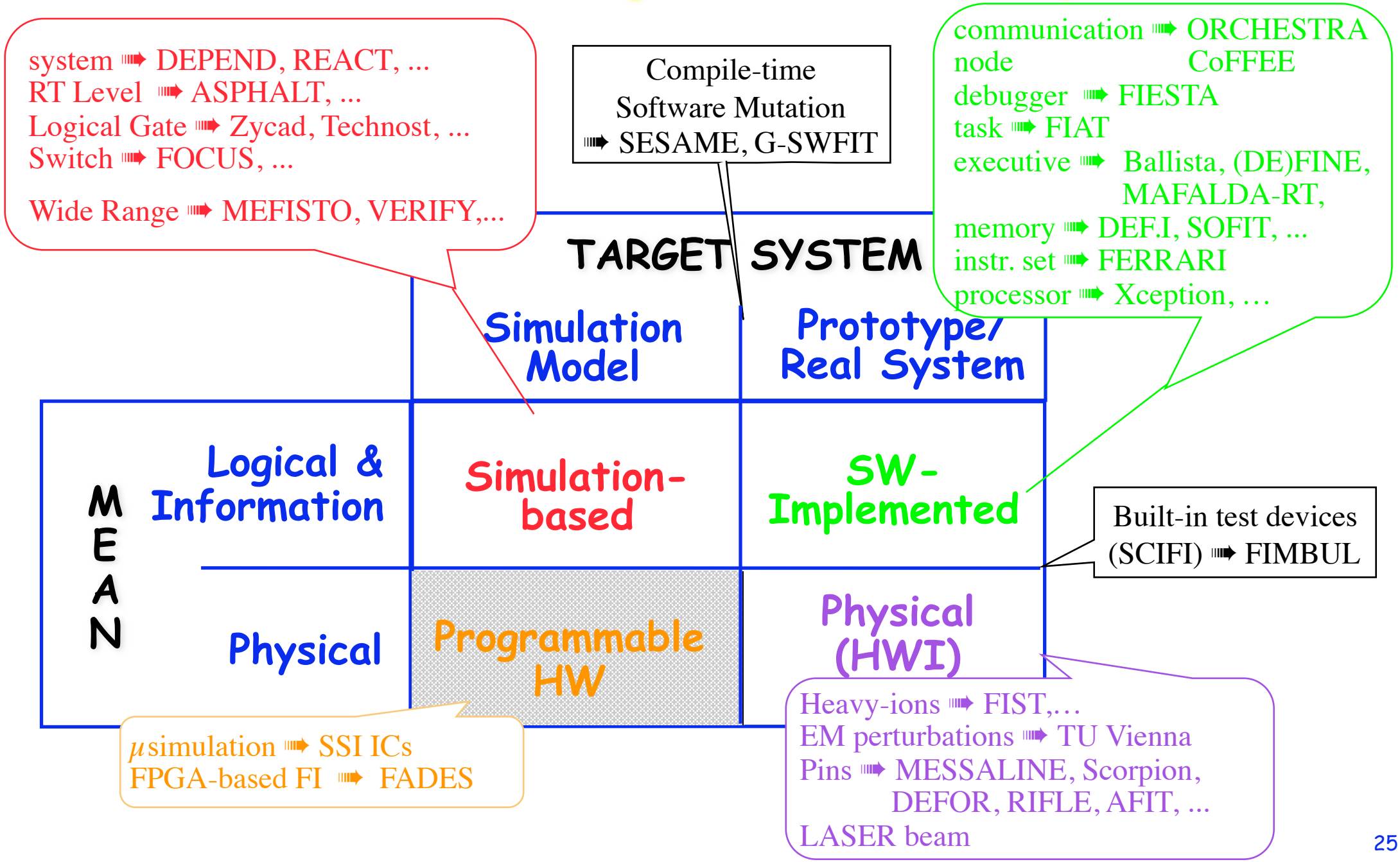
The Fault Injection Attributes: *FARM*



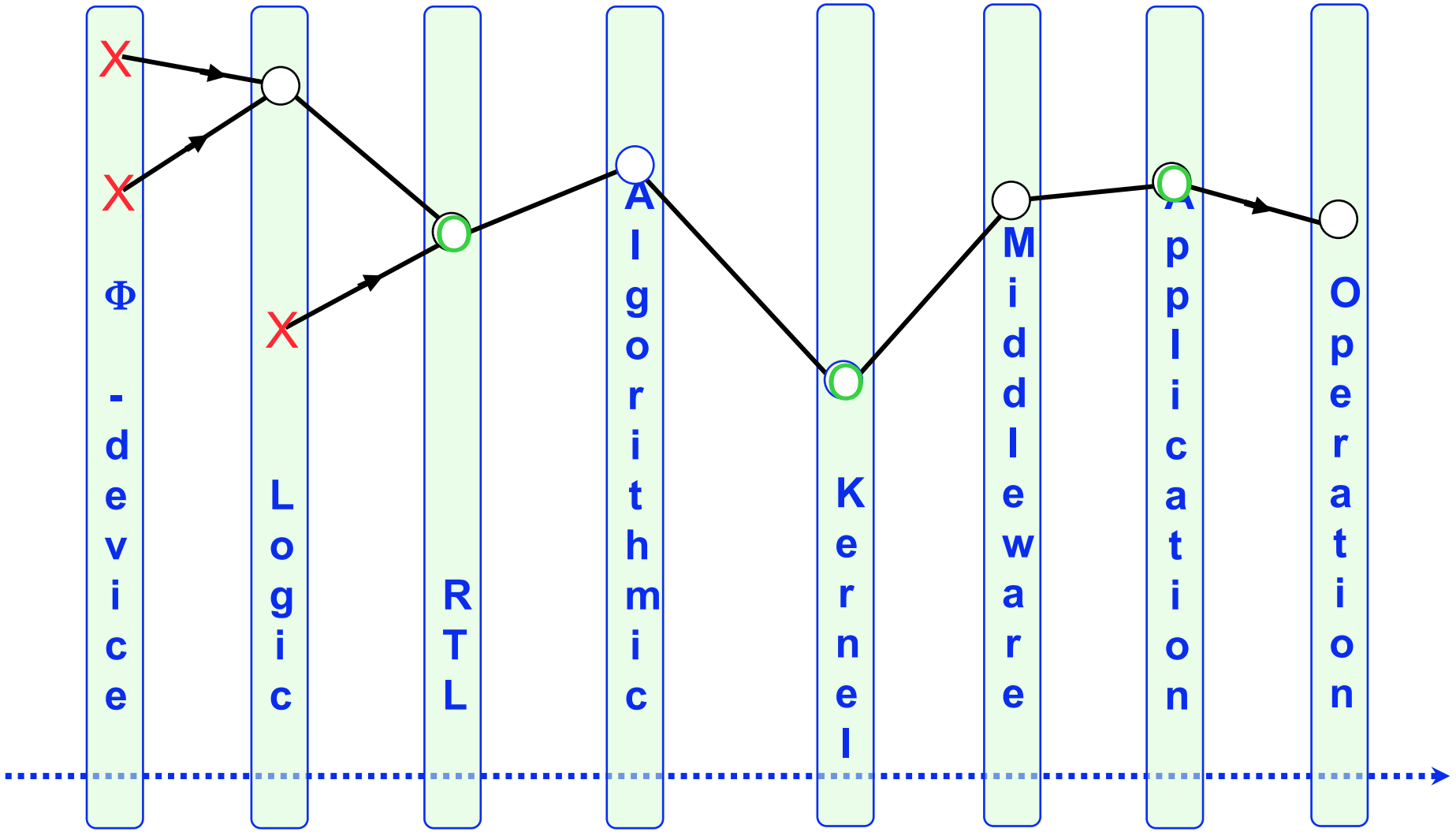
The Fault Injection Techniques



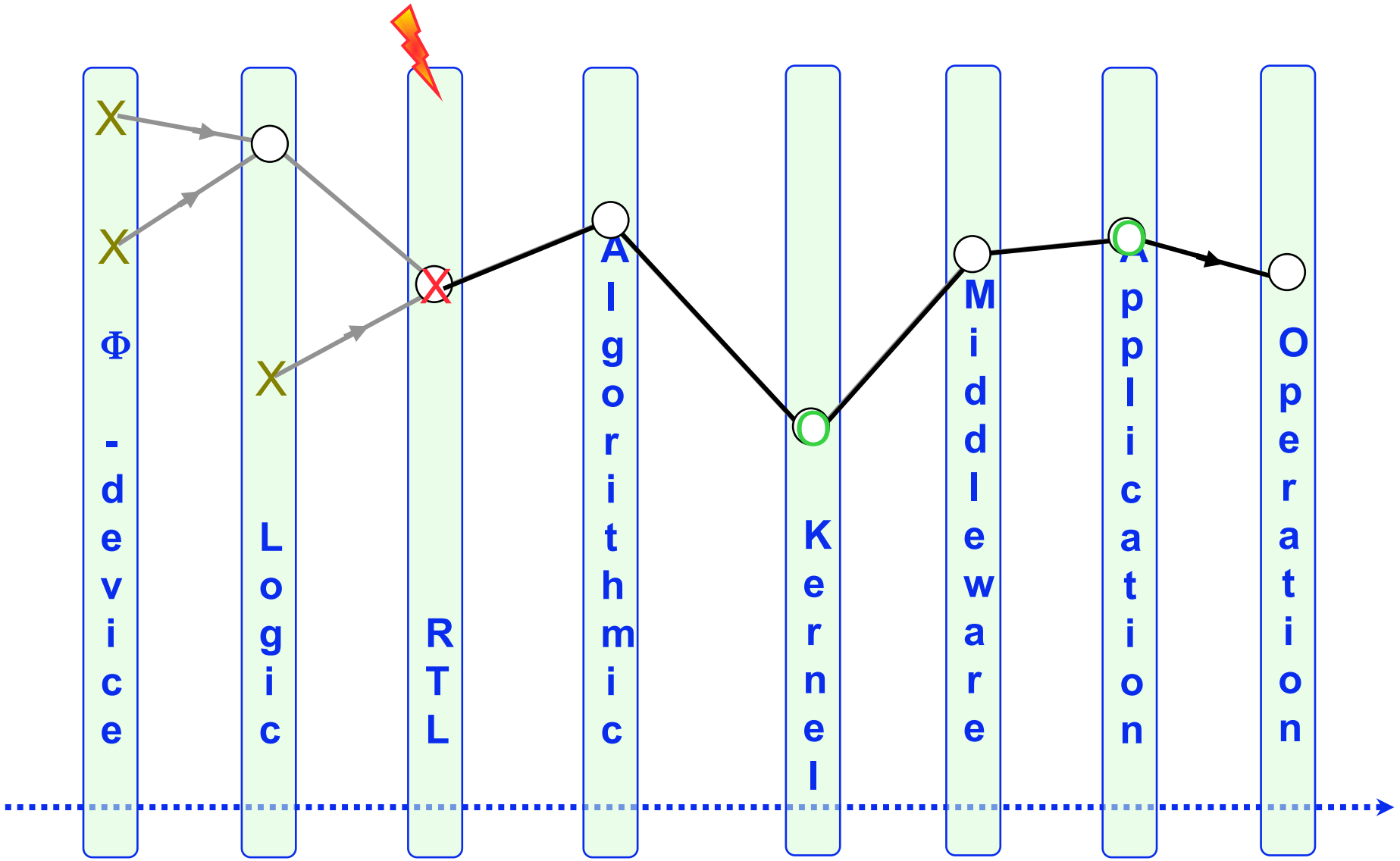
The Fault Injection Techniques



Target System Levels and Fault Pathology

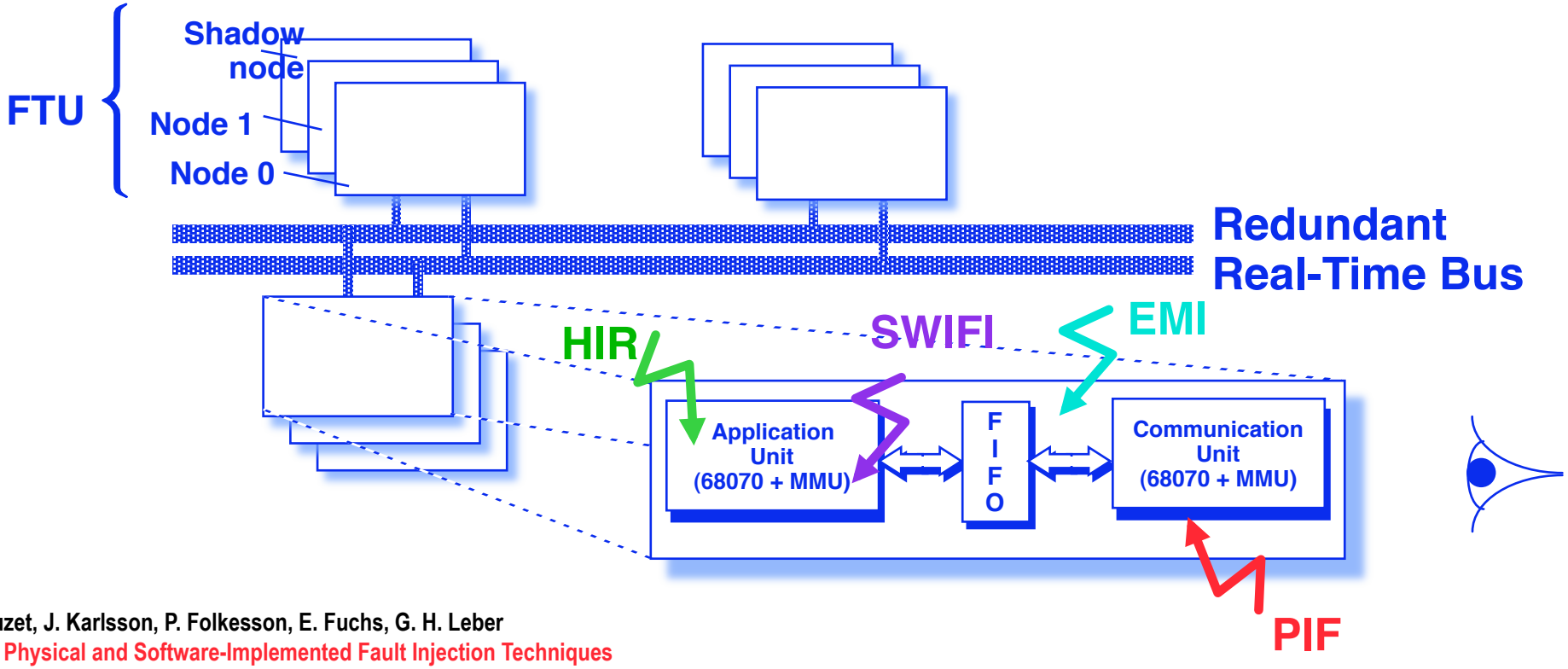


Target System Levels and Fault Pathology



FI Experiments on MARS: Dual Objectives

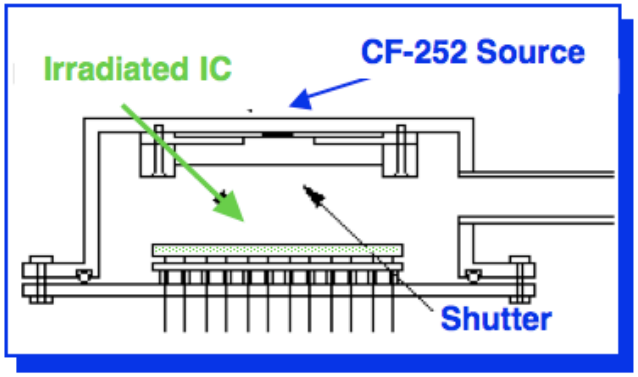
- Extensive Assessment of the "Building Block" of the *VUT MAintainable Real-time System (MARS)* FT Architecture: *the Fail-Silent Node*
- Compare the 4 Fault Injection Techniques Considered (Heavy-Ion Radiations, PIn-Forcing, EMI and Compile-Time SWIFI)



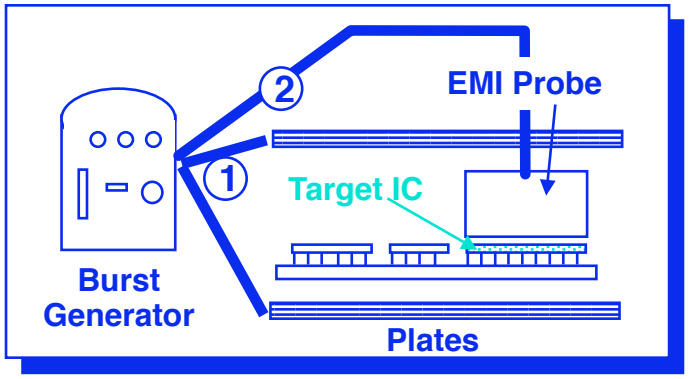
J. Arlat, Y. Crouzet, J. Karlsson, P. Folkesson, E. Fuchs, G. H. Leber
Comparison of Physical and Software-Implemented Fault Injection Techniques
IEEE TC, 52 (9), pp.1115-1133, September 2003

The Fault Injection Techniques

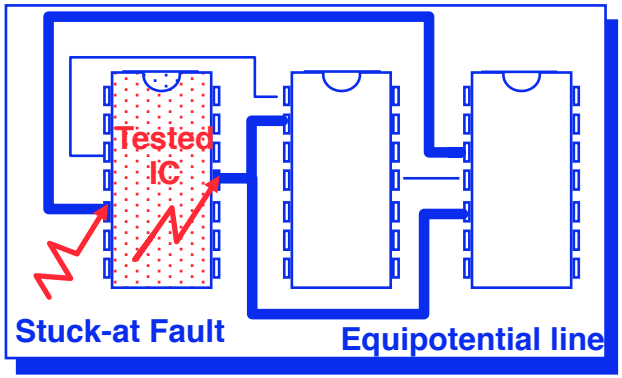
- Heavy-Ion Radiation (HIR)
  + Reachability (Internal IC faults)



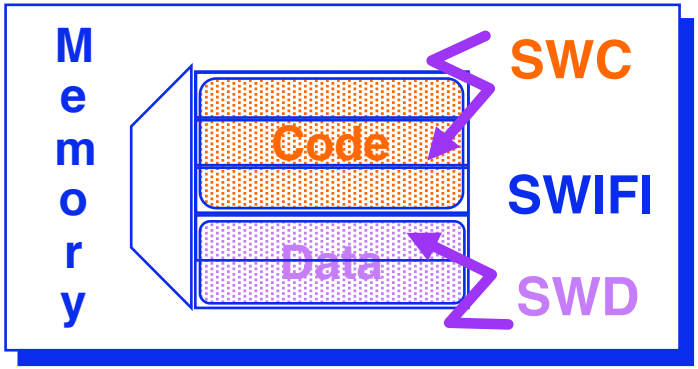
- Electro-Magnetic Interference (EMI)
  + Flexibility (adaption to several systems)



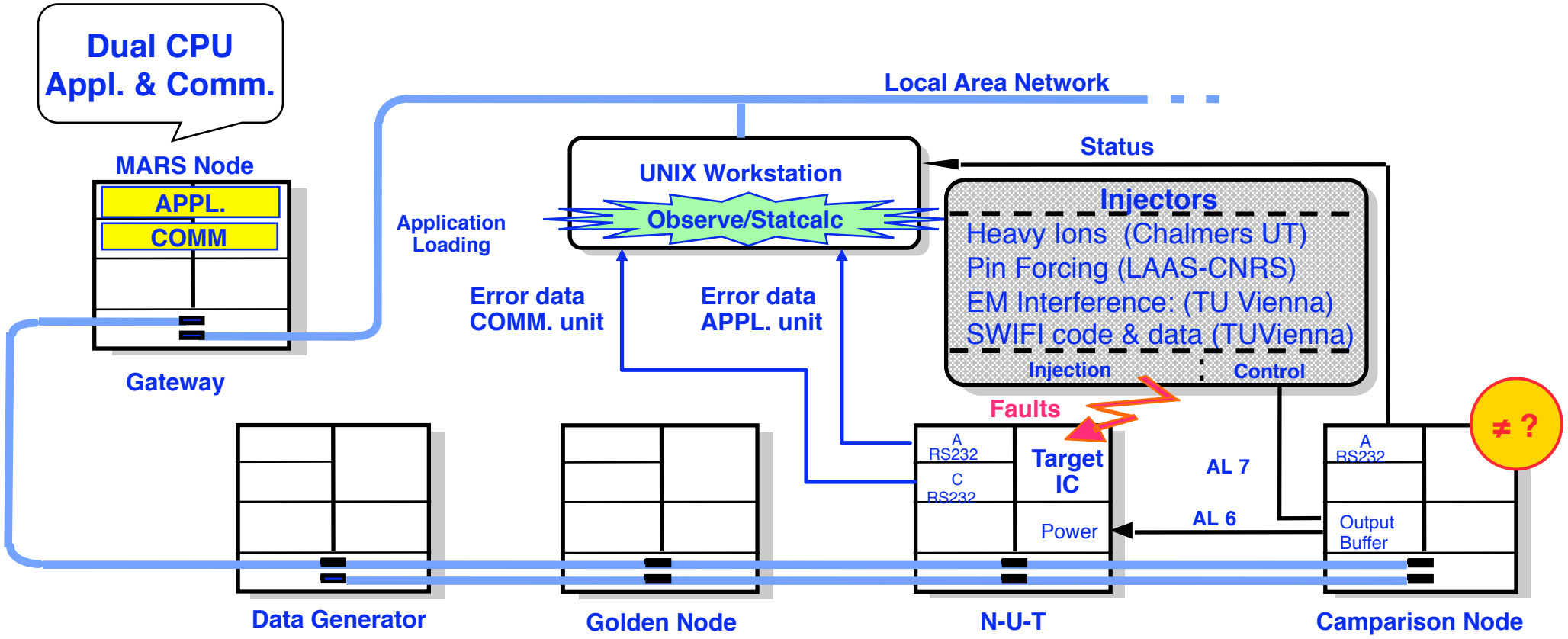
- Pin-level Injection by Forcing (PIF)
  + Controllability
    (distribution among ICs, timing)



- Software-Implemented Fault Injection
  (Compile Time)
  + Ease of application



The Testbed

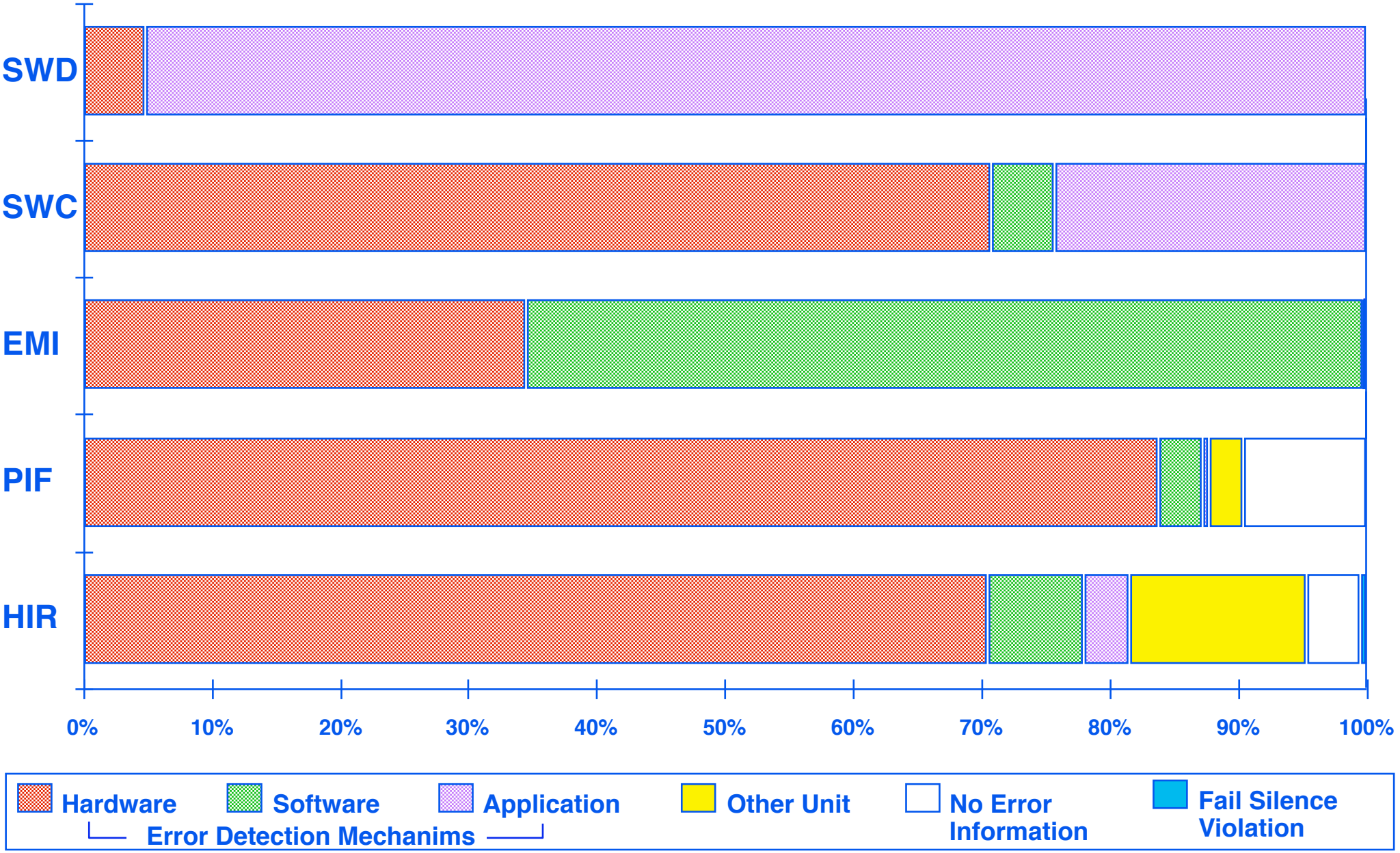

Dual CPU
Appl. & Comm.
Local Area Network
MARS Node
APPL.
COMM
Gateway
Application
Loading
UNIX Workstation
Observe/Statcalc
Status
Injectors
Heavy Ions (Chalmers UT)
Pin Forcing (LAAS-CNRS)
EM Interference: (TU Vienna)
SWIFI code & data (TUVienna)
Injection
Control
Error data
COMM. unit
Error data
APPL. unit
Faults
A
RS232
C
RS232
Target
IC
Power
AL 7
AL 6
A
RS232
Output
Buffer
≠ ?
Data Generator
Golden Node
N-U-T
Camparison Node

The Error Detection Mechanisms (EDMs)

- Level 1 — Hardware
  - CPU: Bus Error, Address Error, Illegal Opcode, Privilege Violation, Zero Divide, etc.
  - NMI: W/D Timer, Power, Parity, FIFO Mngmt, Memory Access, NMI from other Unit, etc.
- Level 2 — Software
  - Operating System (OS): Processing time overflow, various assertions in the OS, etc.
  - Compiler Generated Run-Time Assertions (CGRTA): Value range overflow, etc.
- Level 3 — Application
  - Message Checksum
  - Double Execution (Checksum Comparison)

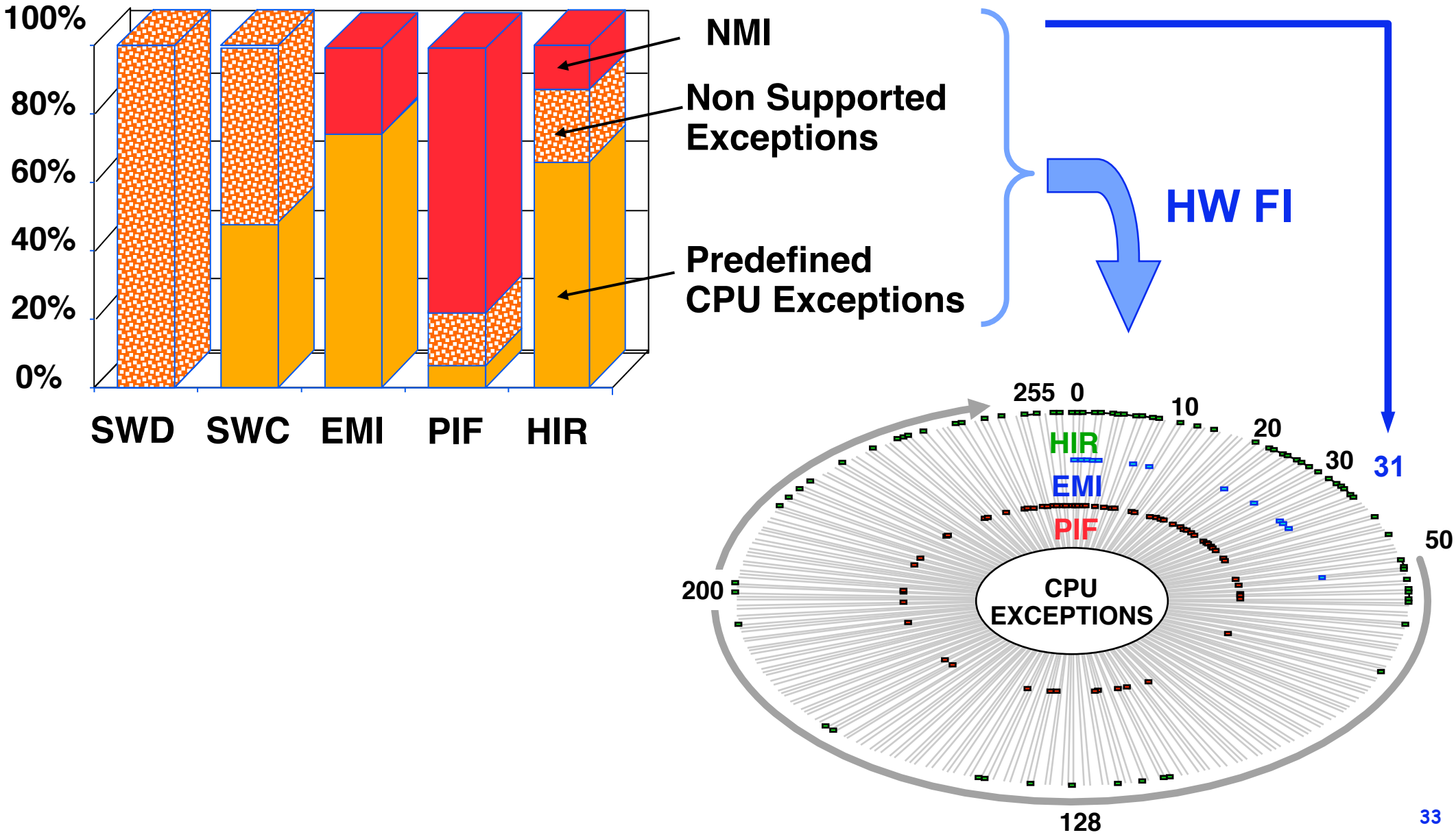
Error Distributions

[All Error Detection Mechanisms Enabled]



Detailed Contribution of HW EDMS

[All EDMs Enabled]



Some Lessons Learned about the Fault Injection Techniques

Properties	Heavy-Ion	Pin Forcing	EMI	CT SWIFI
Reachability	high	medium	medium	low to medium
Controllability wrt Space	low	high	low	high
Controllability wrt Time	none	low to medium	low	medium to high
Repeatability	none to low	medium to high	none to low	high
Reproducibility	medium to high	high	low	high
Non Intrusiveness	low	medium	high	high
Time measurement	low to medium	high	low	medium to high
Efficacy	high	high	high	low

About Fault Model Representativeness

Essential with respect to

- Off-line Testing —> Actual Manufacturing Defects
- Design of Fault-Tolerant Circuits and Systems
  —> Operational faults
- Assessment of the Fault Tolerance

Many Valuable Efforts and Progress made…

But, Still a Challenging Issue!

Acknowledgements

- Organizers of Special Volume and Forum for allowing us to actively participate to the tribute to Christian and, in particular, to recall these pioneering results under the form of such a still "timely historical perspective" ☺
- Many colleagues
  - … at LAAS-CNRS
    - *Jacques Galiay, Alain Costes, Jean-Claude Laprie, Michel Diaz, David Powell, Yves Deswarte, Mohamed Kaâniche, Karama Kanoun*
  - … elsewhere
    - *X. Messonier,P. Rousseau, M. Vergniault (EFCIS)*
    - *J. Karlsson, P. Fokelsson (Chalmers UT)*
    - *H. Kopetz, G. Leber, E. Fuchs (Vienna UT)*
- Christian for his guidance in our first years at LAAS and his continuous friendship along the years!