Formal Specification for Building Robust Real-time Microkernels

Manuel Rodríguez, Jean-Charles Fabre and Jean Arlat

LAAS-CNRS

7, Avenue du Colonel Roche 31077 Toulouse Cedex 4 — France

E-mail: {rodriguez,fabre,arlat}@laas.fr

Abstract

This paper presents a method based on formal specifications for building robust real-time microkernels. Temporal logic is used to specify the functional and temporal properties of real-time kernels with respect to their main services scheduling, (e.g., time. synchronization, and clock interrupts). As an example of a synchronization mechanism, the specification of the Priority Ceiling Protocol is provided. The objective is to verify kernel properties at runtime in order to improve the internal kernel's detection mechanisms and complement their weaknesses. The core of this paper is a complete description of the temporal logic formulas corresponding to real-time kernel specifications. The formulas developed in this paper are the basis for the implementation of fault containment wrappers. The combination of COTS microkernels and wrappers leads to the notion of robust microkernels. The provided case study illustrates the approach on top of an instance of the Chorus microkernel.

1 Introduction

The use of commercial-off-the-shelf (COTS) real-time microkernels is today a target objective for the designers of safety-critical systems, mainly for economic reasons. However, the main worry of the designers is the correctness of this vital component. Providing a solution to guarantee that the preferred candidate fulfills the expected specifications is of very high interest for system integrators. The expression of the specifications using formal methods increases very much the confidence one can have in the final result. Indeed, formal methods are widely used as a mathematical support for the specification and the verification of systems, as well as for the synthesis of implementations whose correctness is then given by construction. The main contribution of this paper is the ability to combine both formal methods and error detection mechanisms for building fault tolerant systems based on robust real-time microkernels.

The approach proposed aims at providing formal specifications for building robust real-time microkernels. The specifications describe properties that are independent of any actual implementation of a given real-time kernel. Temporal logic is used as the specification language, since it constitutes a good framework for expressing both functional and timing properties of systems, as stated in [1]. Properties of realtime kernels are specified with respect to their main services (e.g., scheduling, time, synchronization, and clock interrupts). As an example of a synchronization mechanism, we provide the specification of the Priority Ceiling Protocol [10]. The set of temporal logic formulas can be verified at runtime and the violation of a formula is interpreted as the detection of an error of the kernel. The on-line verification of properties can thus be viewed as a fault containment wrapper based on formal expressions. This approach efficiently combines both an abstract model of the expected behavior of the kernel, as well as error detection mechanisms for hardening the microkernel.

The basic assumption is to consider the microkernel as a finite state machine, as stated in [2]. However, to practically verify kernel properties, it is necessary to reduce the complexity of the model. Our approach consists in defining a nondeterministic, abstract finite state machine (AFSM) of the candidate microkernel, which avoids the so-called state explosion problem [3]. This is viable because the detailed functionality of some parts of the kernel behavior are irrelevant to the properties that need to be checked.

Transitions among states of the AFSM are defined by a number of microkernel events, which are triggered by the kernel execution flow, the kernel environment and the real-time clock. Microkernel events correspond to both external stimuli and the start or termination of actions. The kernel environment can be viewed as being composed of the *user tasks*, which issue system calls, the *real world*, which generates asynchronous inputs, and the *hardware*, which raises interrupts and exceptions (e.g., internal error detection).

The runtime verification of the kernel's properties, with respect to its AFSM, is performed by a model checker, which interprets on-line the temporal logic formulas. The model checker implements a required subset of the temporal logic. In practice, the model checker is implemented as an external module that needs to access internal data and events of the kernel. In short, the model checker is responsible for both the verification of the kernel behavior at runtime, as well as the detection of errors. The description of the model checker is beyond the scope of this paper.

A number of works have been published on the application of formal methods to microkernels. For instance, in [4], a restricted Ada 95 runtime support is specified, together with a minimal model of the system, using a version of RTL expressed in PVS. In [5], some kernel services are specified in VDM, and then compared to a less abstract specification of a simple kernel written in Modula2. In [6], the Z notation is chosen to specify the behavior of the scheduler and interrupt handling components of a kernel for a diagnostic X-ray machine. These works are mainly intended to provide a formal description of the kernel which would replace its ambiguous documentation, and also aim at analyzing kernel properties that may help errors to be detected at early stages in the design process of the system, or in an actual implementation of the kernel. A very interesting architectural model for safety kernels is proposed in [2]. It suggests supplying the kernel with an interface implemented in Ada95 that offers safety services to critical applications. Such an interface is the result of successive refinements from the specification in RTL and Z of safety invariants defined by the applications.

However, to our knowledge, no published work has focused on formal specifications for the runtime verification of the correctness of real-time microkernel services. The runtime verification of formal expressions is a major step forward of our previous work done for the hardening of COTS microkernels for the development of efficient fault tolerant-systems [7]. This work investigated wrappers based on executable assertions instead of formal specifications and it did not consider temporal aspects. The main benefit of the formal specifications described in this paper is two-fold: (i) the formal expressions based on temporal logic express the detailed behavior of a real-time kernel in both time and value domains, (ii) they can be tuned according to the needs and dynamically verified at runtime by a model checker. The combination of both formal specifications and the corresponding model checker can be seen as an extended error detection wrapper.

This paper is organized as follows. Section 2 describes how temporal logic can be extended to specify microkernel services. The specification of an abstract kernel is provided in Section 3, modeling the scheduling, time, synchronization, and clock interrupt services. Verification issues are illustrated in Section 4, regarding the timing properties of an instance of the Chorus microkernel. Finally, Section 5 concludes the paper.

2 Temporal logic for the specification of kernels

Temporal logic [8] is a useful formalism to describe both functional and temporal properties of systems. However, some extensions must be provided so that it can effectively be used to specify kernels. This section presents the temporal logic used for the kernel specification developed in Section 3. The syntax and semantics of the logic are first described, as well as the microkernel events necessary for the specification. The definition of discrete time in kernels is then developed. Finally, additional derived operators and the subset of the temporal logic used are described.

2.1 Syntax and semantics

Temporal logic formulas are built from predicates. A predicate describes or checks the state of the system at a particular instant in time. Predicates are composed of a number of expressions. Expressions are made up of:

- Constants (C): They comprise integer numbers (..., -1, 0, 1, ...).
- Variables (\mathcal{D}) : They may be either a general variable (e.g., th_a , which refers to a thread identifier, *period*, which refers to a time interval, etc.) or a state variable. By convention, state variables are enclosed in square brackets. Some examples are:
 - [Running]: the currently running thread.
 - [Flow]: the current execution flow of the kernel.
- Functions, $f(e_1, ..., e_k)$, where $e_1, ..., e_k$ are expressions: Functions may be i) arithmetic operators (e.g., +, -), ii) state functions, e.g.:
 - prio (tha): the priority of thread tha.
 - highest ([ReadyQueue]): the highest priority thread in the ready queue.

and also iii) *microkernel events*. Microkernel events are explained in Section 2.2. Yet, let us give some examples:

- *Îsignal (th)*, beginning of thread *th* entering the ready queue.
- *icontext_switch*, end of a context switch operation.
 Inductively, formulas (7) are built as follows:
- Predicates, p(e₁, ..., e_k), where e₁, ..., e_k are expressions: Predicates include the relational operators (e.g., =, <, >, ≤). For example:
 - prio $(th_b) < prio (th_a)$: is the priority of thread th_b lower than the priority of thread th_a ?
 - [Running] = th_a : is thread th_a currently running?
 - [Flow] = $\hat{1}$ SetTimer (tm_{a} , abs, period): does the execution flow correspond to the beginning of system call SetTimer, where timer parameter is equal to tm_a , absolute start time is abs, and timer period is period?

• Predicates combined with logical operators (e.g., \neg , \land) and temporal operators, such as Always (\Box), Next (O), and *Sometime* (\Diamond) . For instance, the formula

 $\Box [[ReadyQueue] \neq \emptyset] \land O [[Flow] = \hat{s}ignal (th_a)$ $\wedge O[[Running] = th_a]]$

is true iff the ready queue always contains at least one thread, and at the next instant of time the execution flow corresponds to thread th_a entering the ready queue, which some time later is elected to run.

The truth of a temporal logic formula is given with respect to a model defined by the triple $(\mathcal{D}, \Sigma, \mathcal{H})$, where:

- \mathcal{D} is the data domain. We take \mathcal{D} to be the set of integer numbers, since all the microkernel variables can be represented by an integer. Non integer variables, such as structs, can be easily reduced to an integer.
- Σ is the set of microkernel states. Σ is defined by the set of all possible values taken by the microkernel variables at any instant of time. A state is a tuple of type \mathcal{D}^{4} , where k is the number of variables handled by the microkernel.
- *W* is an interpretation, giving meaning to every function and predicate symbol, i.e.:
 - Let f be a function symbol, then:

 $\mathcal{M} \parallel f \parallel \in (\mathcal{D}^4 \to \mathcal{D})$

- Let p be a predicate symbol, then: $\mathcal{H} \parallel p \parallel \in (\mathcal{D}^{4} \rightarrow \{ true, false \})$

Let σ be an interval of states in Σ^+ , the set of nonempty, finite sequences of states. Let $|\sigma|$ be the length of σ , by convention equal to the number of states of σ minus one. The individual states of an interval σ are denoted by $\sigma_0, \sigma_1, ..., \sigma_{i\sigma}$. The truth of a temporal logic formula is given with respect to an interval σ , where the first state of the interval (i.e., σ_0) refers to the current time, and successive states refer to successive instants of time. Let $C \in \mathcal{C}$, $V \in \mathcal{V}$, and $G, H \in \mathcal{P}$. Accordingly, $\sigma_0 ||V||$ corresponds to the value of the variable V at the current time. The semantics of an interpretation *W* for a given interval σ , is as follows:

- 1. $\mathcal{M}_{\sigma} \parallel \mathbb{C} \parallel = \mathbb{C}$
- 2. $\mathcal{M}_{\sigma} \parallel \mathbb{V} \parallel = \sigma_0 \parallel \mathbb{V} \parallel$

3.
$$\mathcal{M}_{\sigma} || f(e_1, ..., e_k) || = \mathcal{M}_{\sigma} || f || (\mathcal{M}_{\sigma} || e_1 ||, ..., \mathcal{M}_{\sigma} || e_k ||)$$

4.
$$\mathcal{M}_{\sigma} || p(e_{1}, ..., e_{k}) || = \mathcal{M}_{\sigma} || p || (\mathcal{M}_{\sigma} || e_{1} ||, ..., \mathcal{M}_{\sigma} || e_{k} ||)$$

5.
$$\mathcal{M}_{\sigma} \parallel \neg G \parallel = \neg \mathcal{M}_{\sigma} \parallel G \parallel$$

6. $\mathcal{M}_{\sigma} \| \mathbf{G} \wedge \mathbf{H} \| = \mathcal{M}_{\sigma} \| \mathbf{G} \| \wedge \mathcal{M}_{\sigma} \| \mathbf{H} \|$

7.
$$\mathcal{M}_{\sigma} \parallel O G \parallel = \mathcal{M}_{\sigma} \parallel G \parallel$$

- 8. $\mathcal{M}_{\sigma} \parallel \bigcirc G \parallel = \mathcal{M}_{\sigma_{i},...,\sigma_{|\sigma|}} \parallel G \parallel, \forall i \leq |\sigma|$ 9. $\mathcal{M}_{\sigma} \parallel \diamondsuit G \parallel = \neg \mathcal{M}_{\sigma} \parallel \bigcirc \neg G \parallel$

For instance, an interval satisfies $G \wedge H$ if it satisfies both G and H (line 6), and it satisfies Next G (line 7) if G is true at the next instant of time, i.e., if the interval obtained by removing the first state of the interval satisfies G.

2.2 Microkernel events

A microkernel event denotes the current execution flow of the kernel. They can be viewed as markers corresponding to changes of the kernel state, triggered by both external stimuli and the start or termination of actions. Clock interrupts, entering a kernel function, or completing a context switch, are examples of events. The set of events needed for the specification developed in Section 3 is given in Table 1.

	Syscall	Internal
Scheduling		Tsignal (th) ↓context_switch Twait Tyield (th)
Process mgt.	1Create (th) 1Relinquish ↓Relinquish 1Delay (ticks)	1waitFromDelay
Synchro nization	Take (cs) ↓Take (cs) TGive (cs) ↓Give (cs)	↓winlock (th) ↓_winlock (th)
Time mgt.	1SetTimer (tm, abs, period)	↓TimeoutSet (tm, ticks) ↓TimeoutCancel (tm)

Table 1 Microkernel events

Events have been classified by functional component of the microkernel (scheduling, process management, synchronization, and time management). Those events that are triggered by a particular system call handler are referred to as syscall events. Otherwise, they are considered as being internal events.

All syscall events correspond to the start or termination of a system call handler.

For example:

- *Create (th)*: Start of the system call handler for the creation of a new thread th.
- The lay (ticks): Start of the handler that delays the running thread for ticks units of time.
- $\sqrt{Take (cs)}$: Termination of the handler that controls accesses to critical section cs.
- *SetTimer (tm, abs, period)*: Start of the handler that sets timer tm, with period period, and absolute start time abs.

The semantics of some internal events is described hereafter (see also Section 2.1):

- \hat{T} wait: The running thread requests to exit the ready queue.
- *fyield (th)*: Start of thread *th* voluntarily changing of place in the ready queue.
- *Jwinlock (th)*: Thread *th* gains the lock for a critical section.

The description of other microkernel events is explicitly skipped here. A thorough explanation is provided in Section 3.

2.3 Definition of discrete time in a microkernel

Two types of scheduling can be identified: tick driven and event driven, as stated in [9]. Microkernels manage time differently, depending on which type of scheduling they use. Tick (or timer-driven) scheduling based microkernels use a periodic clock interrupt. At every clock interrupt (e.g., every 10 ms), a handler is in charge of performing a number of tasks, such as updating the system time, looking for elapsed timers, moving threads from a delay queue to the ready queue, etc. Discrete time is thus given by such a periodic clock interrupt. In contrast, event scheduling based microkernels explicitly program the hardware timer to interrupt the system at the next closest timeout. In this case, discrete time is given by each count of the hardware timer (e.g., 1 µs between two counts). This paper adopts the convention of referring to each instant of discrete time (i.e., periodic clock interrupts or hardware timer counts) as tick.

In fact, a tick can be viewed as another type of event. Tick events are synchronous, while the other microkernel events are asynchronous. A given tick may match the elapsed time of an on-going timer, whose expiration is managed by the kernel by executing a timeout handler. Let us define two more events. Event $\hat{t}tick$ denotes the occurrence of a tick. If a timeout is triggered at a given tick, then event $\hat{t}tick$ denotes the end of processing of the related timeout handler. If no timeout occurs, then both $\hat{t}tick$ and $\hat{t}tick$ denote the same instant of time. We assume that a timeout handler finishes within its tick interval.

Since we are only interested in ticks leading to a timeout, we can revise the definition of microkernel states (Σ). Accordingly, Σ will be made up of the instantaneous values of the microkernel variables at the occurrence of either a timeout or an asynchronous event. Subsequent computation steps modifying the kernel variables are thus not to be considered, which significantly reduces the number of states.

2.4 Notation

This section presents some additional derived temporal operators and the subset of the temporal logic used for the kernel specification developed in Section 3.

The temporal operators *Next* and *Sometime* have been extended, as explained hereafter:

- $Next_{flick}^{i}$: Refers to the next *i*-th $\hat{f}tick$ event.
- $Next_{Jtick}^{i}$: Refers to the next *i*-th $\int tick$ event.
- Next_{event}ⁱ: Refers to the next *i*-th asynchronous event.
- Next_{event} {evGroup}: Refers to the next asynchronous event from those of the set {evGroup}.
- Sometime^{<i} (p): Refers to some instant in the future before the occurrence of *i î*tick events.

The use of these operators is illustrated in Section 3.

The specification uses a subset of the temporal logic. Let p and q be temporal logic formulas, as defined in Section 2.1. The specification is compliant with the following restrictions:

- Sometime is always guarded by an event, for example: Sometime ([Flow] = $\widehat{1SetTimer \land p}$) where p is not verified until the occurrence of $\widehat{1SetTimer}$.
- The kernel specification consists of a set of formulas with the following structure:

Always ([Flow] = event $\land p \Rightarrow q$)

which means that the verification of q is not carried out until the occurrence of *event*, as long as p is true, where *event* is one of the microkernel events given in Table 1, and p, q are temporal logic formulas which do not use the operator *Always*. The term $[Flow] = event \land p$ is the *antecedent*, which can be thought of as supplying the input or stimulus, whereas the term q is the *consequent*, which is the expected behavior of the kernel to the stimulus.

3 Microkernel specification

A microkernel is usually made up of a set of components that provide basic system services, such as scheduling, process management, synchronization, time management, interrupt management, etc. The number of such components varies from one microkernel to another, and most of the times the kernel can be customized so as to be kept as small as possible. The specification of the kernel can thus be made on the basis of these basic components. This paper mainly concentrates on the specification of scheduling, time management, and synchronization, since they are essential services which must be provided by any real-time system. The specification of the real-time clock interrupts is embedded in the temporal logic notation, as explained in Sections 2.3 and 2.4.

The scheduling specification describes the behavior of a general priority-based FIFO-preemptive scheduler (see Section 3.1), commonly used in real-time systems. Real-time tasks usually define a number of timing parameters, such as the period and the deadline, that greatly depend on the correct behavior of the timer service offered by the kernel. The specification of the timer service is developed in Section 3.2. In Section 3.3 we address synchronization services. Two main types of synchronization are supported by any kernel: mutual exclusion between tasks executing user code, and mutual exclusion between tasks executing kernel code. The former gathers user mutexes, condition variables, semaphores, monitors, an also several synchronization protocols for real-time systems. The Priority Ceiling Protocol [10], a common mechanism to synchronize realtime tasks, is specified in Section 3.3.1. Finally, synchronization within the kernel is supplied by kernel mutexes, the scheduler lock, and the interrupts lock, as described in Section 3.3.2.

3.1 Scheduling

The scheduling specification describes the behavior of those system calls which can modify the scheduling of tasks, namely, Create, Relinquish, and Delay. This list is not exhaustive, as we mainly aim at illustrating the approach. Synchronization system calls, like Take and Give, also modify the scheduling but, for the sake of conciseness, they will only be briefly treated in Section 3.3.1.

Consider the request for the creation of a new thread, specified by Create_1 and Create_2:

Create 1

<u>Always</u> [[Flow] = \uparrow Create(th_b) \land th_a = [Running] \land <u>Sometime</u> [[Flow] = $\hat{}$ signal(th_b) \wedge [Running] = th_a \wedge $prio(th_b) \le prio(th_a)] \Rightarrow$ <u>Next</u>event [[Running] = th_a \land th_b \in [ReadyQueue_{prio(thb)}]]]

Create 2

<u>Always</u> [[Flow] = \uparrow Create(th_b) \land th_a = [Running] \land Sometime [[Flow] = 1signal(th_b) ^ [Running] = th_a ^ $prio(th_b) > prio(th_a)] \Rightarrow$ Nextevent [[Flow] = ↓context_switch ∧ tha ∈ [ReadyQueueprio(tha)] ∧ [Running] = thb]]

Whenever a thread th, requests to create a new thread

th_b, the execution flow, denoted by the variable [Flow], enters the kernel handler devoted to the creation of predicate threads, described by the as [Flow] = \uparrow Create (th_b). Some time later, the kernel will initiate the insertion of a newly created thread the in the ready queue (\uparrow signal). If the priority of th_b is lower than or equal to th_a (Create_1), by the occurrence of the next event, the insertion operation is finished, thread that is still running, and the is inserted in the ready queue of its priority. However, if the priority of the newly created

thread th_b is higher than the priority of the running thread th_a (Create_2), at the next event the kernel executes a context switch. As a result, thread tha is preempted and inserted in the ready queue, and th_b is elected as the newly running thread.

A thread that gives up the CPU is specified by Relinquish_1, Relinquish_2 and Relinquish_3:

Relinguish_1

<u>Always</u> [[Flow] = \uparrow Relinquish \land th_a = [Running] \land [ReadyQueue]-th_a $\neq \emptyset \land$ th_b = highest ([ReadyQueue]-th_a) \land prio (th_b) = prio (th_a) \Rightarrow Nextevent [[Flow] = 1yield(tha) ~ [Running] = tha ~ <u>Nextevent</u> [[Flow] = Jcontext_switch ^

 $th_a \in [ReadyQueue_{prio(tha)}] \land [Running] = th_b]]$

Relinguish 2

Always [[Flow] = TRelinquish ^ tha = [Running] ^ [ReadyQueue]-th_a $\neq \emptyset \land$ th_b = highest ([ReadyQueue]-th_a) \land prio (th_b) < prio (th_a) \Rightarrow <u>Next</u>event [[Flow] = \downarrow Relinquish \land [Running] = th_a]

Relinquish_3

<u>Always</u> [[Flow] = \uparrow Relinquish \land th_a = [Running] \land

 $[ReadyQueue] - [th_a] = \emptyset \Rightarrow$ <u>Nexterent</u> [[Flow] = \downarrow Relinquish \land [Running] = th_a]

Relinguish_1 corresponds to the case where there are at least one ready thread of the same priority as the priority of the running thread tha, i.e., the ready queue of tha's priority is not empty. As a result of the relinquish operation, the kernel puts th_a at the end of its ready queue (Tyield) and yields the thread at the head of the queue as the newly running thread. Conversely, if all ready threads are of lower priority (Relinquish_2), th_a exits the relinquish operation (*JRelinquish*) without giving up the CPU. Finally, Relinquish_3 models the hypothetical case where the running thread is the only ready thread in the system (i.e., the idle thread) and decides to relinquish the CPU, being immediately elected to run again.

A thread may decide to delay for a certain time. This is described by Delay_1:

Delav 1

```
<u>Always</u> [[Flow] = \uparrowDelay (ticks) \land ticks > 0 \land th<sub>a</sub> = [Running] \land
Sometime [[Flow] = JTimeoutSet (toa, ticks) ^ [Running] = tha ^
systicks = [SysTicks] ^
  <u>Sometime</u> [[Flow] = \hat{T} waitFromDelay \land [Running] = th<sub>a</sub>]] \Rightarrow
    Nextevent [[Flow] = 1 wait ~ [Running] = tha ~
     <u>Nexterent</u>[[Flow] = \downarrowcontext_switch \land
     toTicks = systicks + ticks - [SysTicks] \land toTicks \ge 0 \land
     tha ∈ [DelayQueuetoTicks] ∧ tha ∉ [ReadyQueue] ∧
```

[Running] = highest ([ReadyQueue]) <u>Nextuictionatest</u> [tha ¢ [DelayQueue] ^ tha ¢ [ReadyQueue] ^ [Running] = highest ([ReadyQueue]) ^

```
Sometime <1 [[Flow] = 1 signal (tha) ^
```

Nextevent [tha ∈ [ReadyQueueprio(tha)]]]]]]]

Whenever the running thread tha requests to delay for ticks¹ units of time (¹Delay (ticks)), the kernel will attach a timeout object to th_a (\downarrow TimeoutSet (to_a, ticks)). A wait operation is then requested from the delay handler (TwaitFromDelay), which will be served by the scheduler (Twait). Eventually, the leaves the CPU (context switch) and enters the delay queue of its priority $(th_a \in [DelayQueue_{toTicks}])$. The number of ticks that th_a should actually wait (toTicks+1) is calculated in the specification from the instant tha effectively yields the CPU ([SysTicks], i.e., the current system time). When the waiting time is elapsed (Next_{tick}^{toTicks+1}), the clock interrupt handler must have extracted th, from the delay queue. Only some time later within the same tick (Sometime^{<1}), right after the clock handler is exited ([†]signal), th_a should be made ready by the scheduler (tha ∈ [ReadyQueueprio(tha)]).

3.2 Timer management

Timer management provides two main system calls: SetTimer and CancelTimer, specified by Timer_1 and Timer_2, respectively. SetTimer takes as input parameters a timer identifier, tm_a , an absolute start time, *abs*, and a timer period, *period*. Both *abs* and *period* are given in ticks. If the period parameter is null, SetTimer behaves as a watchdog timer or an alarm. Timer_1 uses a number of auxiliary predicates, namely: TooLate, Continue, LostTimeouts and PeriodicTimeout. Their description is given hereafter:

Timer_1

 $\begin{array}{l} \underline{Always} \left[\ [Flow] = \uparrow SetTimer(tm_a, abs, period) \land tm_a \neq \emptyset \land abs > 0 \land period \ge 0 \land th_a = [Running] \land \\ \underline{Sometime} \left[[Flow] = \downarrow TimeoutSet (tm_a, ticks) \land \\ [Running] = th_a \right] \Rightarrow \\ TooLate (tm_a, abs, period) \lor (Continue (abs, period) \land \\ offset = 0 \land LostTimeouts (tm_a, abs, period, offset, 0) \land \\ ticks = abs + offset - [SysTicks] - 1 \land ticks \ge 0 \land \\ tm_a \in [TimeoutQueue_{totks}] \land \\ (\underline{Next}_{10ck}^{abs-offset-(SysTicks]} [tm_a \in [TimeoutQueue_o] \land \\ (period = 0 \lor (period > 0 \land \\ \\ PeriodicTimeout (tm_a, abs, period, period+offset)))] \lor \\ \underline{Sometime}^{cabs+offset, [SysTicks]} [[Flow] = \downarrow TimeoutCancel (tm_a) \land tm_a \notin [TimeoutQueue]])) \right] \end{array}$

TooLate (tm, abs, period)

 $abs \leq [SysTicks] \land period = 0 \land [LostTimeoutCount(tm)] = 1 \land tm \notin [TimeoutQueue]$

Continue (abs, period)

abs > [SysTicks] v period > 0

LostTimeouts (tm, abs, period, offset, lost)

to = abs + offset – [SysTicks] \land ((to > 0 \land [LostTimeoutCount(tm)] = lost) \lor (to \le 0 \land period > 0 \land LostTimeouts (tm, abs, period, period+offset, lost+1))) PeriodicTimeout (tm, abs, period, offset)

<u>Sometime</u>^{<1} [[IntFlow] = ↓TimeoutSet (tm, ticks) ∧ ticks = period ∧ ticks = abs + offset - [SysTicks] ∧ tm ∈ [TimeoutQueue_{ticks}] ∧ <u>(Next</u>_{Ttick}^{period} [tm ∈ [TimeoutQueue₀] ∧ PeriodicTimeout (tm, abs, period, period+offset)] ∨ <u>Sometime</u>^{operiod} [[Flow] = ↓TimeoutCancel (tm) ∧ tm ∉ [TimeoutQueue]])]

A running thread th_a may set a timer tm_a (Timer_1), with absolute start time abs, and period equal to period. However, since the kernel is preemptive, an arbitrary amount of time can passed between the SetTimer request and its completion by the kernel (JTimeoutSet). As a consequence, the absolute start time might become lower than the current time (abs \leq [SysTicks]). In this case, if tm_a behaves as an alarm (period = 0), then it is too late to set the timer (TooLate), and a check is made on whether the kernel notified an error ([LostTimeoutCount(tm)] = 1) and tma was not inserted in the timeout queue (tm ∉ [TimeoutQueue]). Otherwise (Continue), the kernel should set tm_a either at abs (abs > [SysTicks]), or to the next closest period ($abs \leq [SysTicks] \land period > 0$). LostTimeouts checks the number of lost periods, so that the next release time can be computed (ticks = abs + offset - [SysTicks] - 1). Accordingly, the kernel inserts tma in the timeout queue with a timeout value of ticks units of time ($tm_a \in [TimeoutQueue_{ticks}]$). Then, unless the timer is cancelled (*\TimeoutCancel*), it eventually elapses (Next_{Ttick}^{abs+offsel-[SysTicks]}). A check is made right before the timeout handler is executed on whether tm_a is in the timeout queue of 0 ticks $(tm_a \in [TimeoutQueue_0])$. This process is periodically repeated, as specified by PeriodicTimeout, i.e., at every expiration of the period, the clock interrupt handler inserts tma in the timeout queue with a timeout value of period ticks, until it is cancelled.

The specification for *CancelTimer*, **Timer_2**, is the following:

Timer_2

<u>Always</u> [[Flow] = \uparrow CancelTimer (tm_a) ∧ tm_a ∈ [TimeoutQueue] ∧ th_a = [Running] ⇒

Timer_2 expresses that whenever a request to cancel an on-going timer tm_a is issued, some time later, the kernel extracts tm_a from the timeout queue.

3.3 Synchronization

3.3.1 Priority Ceiling Protocol

The Priority Ceiling Protocol (PCP) [10] provides two main system calls, namely: **Take**, to ask for access to a critical section, and **Give**, to release a critical section. The protocol also defines two special queues: the *block queue* ([BlockQueue]), which is a priority-ordered list of threads blocked by the ceiling protocol, and the *lock*

¹ See Section 2.3 for the definition of ticks.

queue ([LockQueue]), corresponding to a list of currently locked critical sections ordered according to their priority ceilings. The specification is given by a number of formulas, describing Take (Take_winlock, Take_1, Take_2), as well as Give (Give_owner, Give_1, Give_winlock, Give_2, Give_3, Give_lock_queue, Give_4, Give_5). Finally, as stated in Section 3.1, Take and Give can also modify the scheduling of tasks. This point is illustrated by Sched_take_2, which is the scheduling version of Take_2.

An auxiliary constant, *t*EvCeiling, and two boolean functions, TakeOccurs and GiveOccurs, have been defined, which are described hereafter:

\$EvCeiling = {1Take, ↓Take, 1Give, ↓Give, ↓winlock, ↓¬winlock }

 $\label{eq:GiveOccurs} \begin{array}{l} GiveOccurs \ (th_a, cs_a) = ([Flow]= \Tilde{Give(cs_a)} \land th_a = [Running] \land \\ [Owner]= th_a \land cs([Owner]) = cs_a) \end{array}$

EvCeiling is a set containing the ceiling events (\uparrow Take, \downarrow Take, \uparrow Give, \downarrow Give, \downarrow winlock, \downarrow -winlock). TakeOccurs expresses that a **Take** operation (\uparrow Take) on a critical section cs_a is permitted only if the ceiling of cs_a is higher than or equal to the static priority of the running thread. GiveOccurs states that a critical section cs_a cannot be released (\uparrow Give) unless the running thread is the owner of the lock ([Owner] = th_a), and the current locked critical section is cs_a (cs ([Owner]) = cs_a).

The operation **Take** is described by **Take_winlock**, **Take_1** and **Take_2**:

Take_winlock

<u>Always</u> [TakeOccurs (th_a, cs_a) ∧ [Owner] ≠ Ø ⇒ <u>Next</u>event^{‡EVCelling} [([Flow] = ↓winlock (th_a) ∨ [Flow] = ↓winlock (th_a)) ∧ [Running] = th_a]]

Take_1

<u>Always</u> [TakeOccurs (th_a, cs_a) \land ([Owner] = $\emptyset \lor$

Take_2

<u>Always</u> [TakeOccurs (th_a, cs_a) \land [Owner] $\neq \emptyset \land$

 $\underline{Next}_{event} \downarrow^{EvCeiling} [[Flow] = \downarrow \neg winlock (th_a) \land [Running] = th_a] \Rightarrow$

<u>Sometime</u> [[Flow] = \uparrow wait \land [Running] = th_a] \rightarrow

 $\frac{Next_{event}}{\wedge th_a} \in [BlockQueue] \land$

 $\neg \exists cs_t \in [LockQueue]: thread (cs_t) = th_a]$]

Take_winlock states that whenever the running thread tha initiates a Take operation on a critical section cs_a , and the lock is not free ([Owner] $\neq \emptyset$), by the occurrence of the next ceiling event (Next_{event} t^{EvCeiling}), either tha has gained the lock (\downarrow winlock), or it has not (\downarrow -winlock). Take_1 expresses that if the lock is free ([Owner] = \emptyset) or

th_a gains the lock (\downarrow winlock), at the next ceiling event th_a exits the **Take** operation (\downarrow Take) being the new owner of the lock ([Owner] = th_a), and also cs_a is inserted in the lock queue (cs_a \in [LockQueue]). On the contrary, **Take_2** specifies that whenever the lock is not free and th_a does not gain the lock, th_a is blocked (\uparrow wait). Hence, by the end of the next context switch, the owner inherits th_a's priority (prio ([Owner]) = prio (th_a)), th_a is inserted in the block queue (th_a \in [BlockQueue]), and also it must be true that th_a was not running within a critical section ($\neg \exists cs_t \in$ [LockQueue]: thread (cs_t) = th_a]).

The specification of **Give** is given by the next formulas:

Give_owner

<u>Always</u> [[Flow] = $\widehat{}$ Give (cs_a) \land th_a = [Running] \Rightarrow [Owner] = th_a \land cs ([Owner]) = cs_a]

Give_1

<u>Always</u> [GiveOccurs (th_a, cs_a) ∧ [BlockQueue] = Ø \Rightarrow <u>Next</u>event ^{tEvCelling} [[Flow] = ↓Give (cs_a) ∧ [Running] = th_a ∧ [Owner] = thread (highest ([LockQueue]))]]

Give_winlock

<u>Always</u> [GiveOccurs (th_a, cs_a) ∧ [BlockQueue] $\neq \emptyset$ ∧ th_b = highest ([BlockQueue]) ⇒

 $\underbrace{Next_{event}}_{[Flow]} \stackrel{\text{TevCeiling}}{=} [([Flow] = \downarrow winlock(th_b) \lor [Flow] = \downarrow winlock(th_b)) \land [Running] = th_a]]$

Give_2

 $\begin{array}{l} \underline{\text{Always}} \left[\begin{array}{l} \text{GiveOccurs} \left(\text{th}_{a}, \text{cs}_{a} \right) \land \left[\text{BlockQueue} \right] \neq \varnothing \land \\ \text{th}_{b} = \text{highest} \left(\left[\text{BlockQueue} \right] \right) \land \text{prio} \left(\text{th}_{b} \right) = \text{prio} \left(\text{th}_{a} \right) \land \\ \underline{\text{Next}}_{\text{event}} \stackrel{\uparrow \text{EvColling}}{=} \left[\left[\text{Flow} \right] = \downarrow \text{winlock} \left(\text{th}_{b} \right) \land \\ \left[\text{Running} \right] = \text{th}_{a} \right] \Rightarrow \\ \underline{\text{Sometime}} \left[\left[\text{Flow} \right] = \uparrow \text{signal} \left(\text{th}_{b} \right) \land \left[\text{Running} \right] = \text{th}_{a} \right] \rightarrow \\ \underline{\text{Next}}_{\text{event}} \left[\left[\text{Flow} \right] = \downarrow \text{context_switch} \land \\ \text{cs} \left(\text{th}_{b} \right) \in \left[\text{LockQueue} \right] \land \left[\text{Qwner} \right] = \text{th}_{b} \land \\ \text{th}_{b} \notin \left[\text{BlockQueue} \right] \land \left[\text{Running} \right] = \text{th}_{b} \right] \end{array}$

Give_3

 $\begin{array}{l} \underline{Always} \left[\begin{array}{l} GiveOccurs \left(th_{a}, cs_{a} \right) \land \left[BlockQueue \right] \neq \varnothing \land th_{b} = \\ & \text{highest} \left(\left[BlockQueue \right] \land prio \left(th_{b} \right) < prio \left(th_{a} \right) \land \\ & \underline{Next_{event}}^{\pm E^{COulling}} \left[\left[Flow \right] = \downarrow winlock \left(th_{b} \right) \land \left[Running \right] = th_{a} \right] \Rightarrow \\ & \underline{Sometime} \left[\left[Flow \right] = \uparrow Signal \left(th_{b} \right) \land \left[Running \right] = th_{a} \right] \rightarrow \\ & \underline{Next_{event}} \left[\left[Flow \right] = \downarrow Give(cs_{a}) \land \left[Running \right] = th_{a} \land \\ & cs \left(th_{b} \right) \in \left[LockQueue \right] \land \left[Owner \right] = th_{b} \land \\ & th_{b} \notin \left[BlockQueue \right] \right] \end{array}$

Give_lock_queue

<u>Always</u> [GiveOccurs (th_a, cs_a) ∧ [BlockQueue] ≠ Ø ∧ <u>Next_{event}^{1EvCelling} [[Flow] = ↓¬winlock] ⇒</u> [LockQueue]-cs_a ≠ Ø ∧ [Running] = th_a]

Give_4

<u>Next_{event}</u> [[Flow] = ↓¬winlock (th_b) ∧ [Running] = th_a ∧ prio (th_b) = prio (th_a)] ⇒ <u>Next_{event}</u> [[Flow] = ↓Give(cs_a) ∧ [Running] = th_a ∧

 $\frac{|Vext_{avent}}{|Owner]} = th_a \land prio ([Owner]) = prio (th_b)]$

Give 5

<u>Always</u> [GiveOccurs (th_a, cs_a) \land [BlockQueue] $\neq \emptyset \land$ $th_b = highest ([BlockQueue]) \land$

<u>Next</u>event^{EvCeiling} [[Flow] = \downarrow -winlock (th_b) \land [Running] = th_a \land prio (th_b) < prio (th_a)] ⇒ <u>Next</u>evert^{1EvCelling} [[Flow] = ↓Give (cs_a) ∧ [Running] = th_a ∧

([Owner] = tha v

 $([Owner] \neq th_a \land [Owner] = thread (highest ([LockQueue]))$ \land prio ([Owner]) = prio (th_b)))]]

Give_owner states that every time the running thread th_a releases a critical section cs_a, th_a must be the owner of the lock and cs_a must be the current locked critical section. Whenever the latter is true and the block queue is empty (Give_1), the owner is equal to the ready thread holding the critical section with the highest priority ceiling ([Owner] = thread (highest ([LockQueue]))). Conversely, if there are threads in the block queue, once cs_a is released, the highest priority blocked thread tries to become the owner (Give_winlock). Give_2 specifies the case where the running thread th_a is blocking a thread th_b (i.e., tha had inherited thb's priority) and thb gains the lock. In this case, th_b is extracted from the block queue (th_b \notin [BlockQueue]), its critical section is inserted in the lock queue (cs (th_b) \in [LockQueue]), and th_b becomes the newly running thread. However, if th_b is being blocked by another thread (and hence th_b's priority is lower than tha's priority, as described by Give_3), tha keeps running. Further on, consider the case where the highest priority blocked thread the does not gain the lock. This means that, apart from cs_a, there is at least one more critical section in the lock queue, as described by Give_lock_queue. If the is blocking the (Give_4), this means that the did not gain the lock because of a nested critical section being locked by tha. Hence, tha remains the owner and enters the nested critical section inheriting th_b's priority. On the other hand, the priority of the blocked thread the might be lower than the's priority, i.e., th_b is not being blocked by th_a (Give_5). In this case, as long as the does not hold any nested locked critical sections, the owner is substituted by the highest priority thread currently executing inside a critical section thread (highest ([LockQueue]))), ([Owner] = which inherits th_b's priority.

Take_2, Give_2 and Give_3 also modify the scheduling state, since they involve a number of scheduling operations, as indicated by events 1 signal, Twait, and \context_switch. Consider Sched_take_2, which is the scheduling version of Take_2:

Sched_take_2

Always [TakeOccurs (tha, csa) ^

- $\underbrace{\text{Next}_{\text{event}}}_{\text{fevCetting}} \text{ [[Flow] = } \downarrow \neg \text{winlock (th}_{a}) \land \text{[Running] = th}_{a} \text{]} \Rightarrow$ <u>Sometime</u> [[Flow] = \uparrow wait \land [Running] = th_a \land
- th_r = highest ([ReadyQueue]-th_a)] \rightarrow
- Nextevent [[Flow] = ↓context_switch ∧ tha ∉ [ReadyQueue] ∧ $[Running] = th_r]$

Sched take 2 has the same antecedent as Take 2. However, its consequent specify the state of scheduling variables (e.g., ReadyQueue), instead of PCP variables.

3.3.2 Internal synchronization

Microkernels use three different kinds of locks for synchronization, namely: mutex locks internal (Mutext_lock), the scheduling lock (Sched_lock), and the interrupt lock (Int_lock). A mutex lock is a binary semaphore of general use, which can be open or closed. It is used to prevent a region in the microkernel from being entered by more than one thread at a time. The scheduling lock is a special mutex that controls access to the scheduling resource. When the scheduling lock is closed, the running thread cannot be preempted. Even though it provides mutual exclusion between threads, it does not prevent interrupts from getting the CPU. Finally, the interrupt lock avoids interrupts from occurring, and is equivalent to disabling interrupts at the processor level. Therefore, Int_lock is the most stringent lock mechanism, whereas Mutex_lock is the least one. This relation can be represented in the following way:

$Mutex_lock \supset Sched_lock \supset Int_lock$

Lock_1, Lock_2, and Lock_3 specify the least stringent lock that the kernel must be using at the occurrence of an event (if needed).

Lock_1

Always [[Flow] =1Take v [Flow] =1Take v [Flow] =1Give v [Flow] =↓Give ∨ [Flow] =↓winlock ∨ [Flow] =↓-winlock ⇒ [Lock] ⊆ Mutex_lock]

Lock_2

Always [[Flow] = \downarrow context_switch \vee [Flow] = \uparrow signal \vee

- [Flow] = 1wait v [Flow] = 1yield v [Flow] = 1Relinquish v
- [Flow] = ↓Relinquish ∨ [Flow] = ↑waitFromDelay ⇒

[Lock] ⊆ Sched_lock]

Lock 3

<u>Always</u> [[Flow] = ↓TimeoutSet ∨ [Flow] = ↓TimeoutCancel ⇒ [Lock] int lock]

Lock_1 specifies than whenever Take, Give (both start and ending), \downarrow winlock, or \downarrow -winlock events occur, the kernel must be at least running under the mutex lock, but it could also be running under the scheduling or interrupt locks. Lock_2 encompasses those events whose corresponding actions use some scheduling-related data, as the priority of the running thread. Hence, the scheduling events (*context_switch*, *signal*, *wait*, and \uparrow yield), and other events, such as \uparrow Relinguish, ↓Relinguish, and ↑waitFromDelay, require preemption to be disable. Finally, ↓TimeoutSet and ↓TimeoutCancel (Lock_3) are triggered from the clock interrupt handler, which accesses time-related queues (e.g., the TimeoutQueue), so interrupts are required to be disabled (specially the clock interrupt, which is the highest priority interrupt).

4 Verification of the timer properties

To illustrate the verification and fault tolerance capabilities offered by the specification, an instance of the Chorus/ClassiX r3.1 microkernel [11] has been verified against the timer properties defined in Section 3.2 (Timer_1 and Timer_2). The workload used is a general periodic task, τ_A , whose pseudo-code is shown in Figure 1.

1.	task body Thread is
2.	begin
3.	Initialize ();
4.	<pre>set_timer (tm, t_{ABS}, T);</pre>
5.	loop
6.	<pre>wait_next_release ();</pre>
7.	<pre>Periodic_Code ();</pre>
8.	end loop;
9.	end Thread;
	Figure 1. Periodic task

The task first initializes (line 3) and executes the set_timer system call, which requests to the kernel to set a periodic timer tm, with absolute start time t_{ABS} , and period equal to T (line 4). Next, it enters a loop where the task first suspends until its next release (line 6) and then executes its periodic code (line 7). Each release of the task is referred to as *instance* (I_i).

Suppose that a higher priority task, τ_B , preempts task τ_A while it is executing set_timer, i.e., before the call returns. Tasks τ_A and τ_B have been run on Chorus² along with the timer formulas, and the messages issued during their verification are shown in Figure 2.

At time t₂, the kernel computes the first release time of τ_A , namely, Δ , as the difference between t_{ABS} and the current time t₂. Unfortunately, task τ_A is preempted at time t_2 , right after the kernel has computed Δ . As a result, once τ_A resumes at t₃, the kernel works out τ_A 's first release as the current time t₁ plus Δ . This means that τ_A 's instances are executed out of pace. This behavior leads to the violation of Timer_1 at time t₃, as shown in lines 9 and 17, which can be viewed as the detection of a kernel error. Line 9 notifies that Δ (labeled as delta in Figure 2) has been given an erroneous value, whereas line 17 (some microseconds later) warns about timer tma being inserted in an incorrect timeout queue. The verification of the timer properties in Chorus allows this behavior to be successfully detected. Otherwise, if not taken into account, such a behavior is prone to cause missed deadlines or inexplicable delays in data transmission.

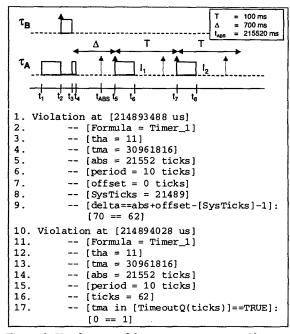


Figure 2. Verification of the timer properties in Chorus (Note that the diagram is not to scale)

As illustrated in this section, our approach provides error detection in the time domain. It is worth noting however that error recovery mechanisms could also be implemented to let the kernel run in a graceful degraded mode. From a performance point of view, the overhead of verifying **Timer_1** on task τ_A was 232 µs. Further measurements are currently being carried out, but the first results obtained show that the overhead is limited.

5 Conclusion

In this paper, we have provided a method for building robust real-time microkernels based on formal specifications. The specifications consist of an abstract model of the kernel behavior that describes some of the essential services offered by any real-time kernel, namely, scheduling, time, synchronization, and clock interrupt management. Kernel services and their corresponding properties are specified in temporal logic. The specification is split into a set of temporal logic formulas that can be verified at runtime. The violation of a formula entails the detection of an error, which can further lead to error recovery actions so as to put the kernel in a safety state. Actually, the specification and the related model checker correspond to a functional and timing wrapper of the kernel. A microkernel encapsulated with such a wrapper leads to the notion of robust real-time microkernel. A very positive aspect of the method is also that such wrappers can be easily customized and ported to various COTS microkernels.

² set_timer and wait_next_release correspond to timerSet and timerThreadPoolWait in Chorus, resp.

The specification presented in this paper is being extended and used for the verification and hardening of microkernels, presently the Chorus/ClassiX microkernel as a first target candidate. The efficient implementation of wrappers based on formal specifications is also a current subject of research. From our first experiments, the overhead introduced by the verification of the temporal logic formulas by the runtime model checker is very limited. Moreover, this overhead can be taken into account in the design of upper level real-time applications, i.e., included in the real-time development process. It is worth noting that we are also addressing issues concerning the impact of wrappers in both hard and soft real-time systems, where predictability and performance are of primary importance. The assessment of the robustness of the resulting microkernels encapsulated with formal wrappers will be done using fault injection techniques [12] and tools [13].

Finally, the method and the experimental fault injection environment will be used to improve and assess the robustness of other real-time kernels currently used in industrial safety critical systems, in particular in the avionics domain.

Acknowledgements. Manuel Rodríguez is supported by Thomson-CSF (SODETEG). The work reported in this paper was carried out in the framework of LIS³. Thanks go to Scott Hazelhurst (Wits University, South Africa) who provided useful insights on temporal logic in the early phase of this work, during his stay at LAAS. Comments from François Scheerens (SODETEG) are gratefully acknowledged.

References

- S. Hazelhurst, J. Arlat, "Specifing and verifying faulttolerant hardware", France-South Africa Cooperation, LAAS report No99514, 1999.
- [2] A. Burns, A. J. Wellings, "Safety Kernels: Specification and Implementation", *High Integrity Systems*, vol. 1, no. 3, pp. 287-300, 1995.
- [3] S. Edwards, L. Lavagno, E. A. Lee, A. Sangiovanni-Vincentelli, "Design of Embedded Systems: Formal Models, Validation, and Synthesis", *Proceedings of the IEEE*, vol. 85, no. 3, pp. 366-390, 1997.
- [4] S. Fowler, A. J. Wellings, "Formal Analysis of a Real-Time Kernel Specification", 4th International Symposium on Formal Tecniques in Real-Time and Fault Tolerant Systems, 1996.

- [5] J. Gorski, A. Wardzinski, "Formal Specification and Verification of a Real-Time Kernel", Proceedings of 6th Euromicro Workshop on Real-Time Systems, pp.205-211, 1994.
- [6] J. M. Spivey, "Specifying a Real-Time Kernel", IEEE Software, vol. 5, no. 7, pp. 21-28, September 1990.
- [7] F. Salles, M. Rodríguez, J.-C. Fabre, J. Arlat, "MetaKernels and Fault Containment Wrappers", 29th IEEE International Symposium on Fault-Tolerant Computing (FTCS-29), pp. 22-29, Madison, Wisconsin, USA, 1999.
- [8] S. Hazelhurst, C.-J. H. Seger, "Symbolic Trajectory Evaluation", in Formal Hardware Verification: Methods and Systems in Comparison, State of the Art Survey Lecture Notes in Computer Science 1287, T. Kropf, Ed.: Springer-Verlag, pp. 3-79, 1997.
- [9] N. C. Audsley, A. Burns, R. I. Davis, K. W. Tindell, A. J. Wellings, "Fixed Priority Pre-emptive Scheduling: An Historical Perspective", *Real-Time Systems*, vol. 8, no. 3, pp. 173-198, 1995.
- [10] L. Sha, R. Rajkumar, J. P. Lehoczky, "Priority Inheritance Protocols: An Approach to Real-Time Synchronization", *IEEE Transactions on Computers*, vol. 39, no. 9, pp. 1175-1185, 1990.
- [11] Chorus, "Chorus/ClassiX r3 Technical Overview", Technical Report CS/TR-96-119.8, Chorus Systems, 1996.
- [12] J.-C. Fabre, F. Salles, M. Rodríguez, J. Arlat, "Assessment of COTS Microkernels by Fault Injection", 7th IFIP International Working Conference on Dependable Computing for Critical Applications (DCCA'99) - Can we rely on computers?, San Jose, California, USA, 1999.
- [13] M. Rodríguez, F. Salles, J.-C. Fabre, J. Arlat, "MAFALDA: Microkernel Assessment by Fault Injection and Design Aid", 3rd European Dependable Computing Conference (EDCC-3), Prague, Czech Republic, 1999.

³ Located at LAAS, the Laboratory for Dependability Engineering (LIS) was a Cooperative Laboratory between five industrial companies (Aerospatiale Matra Airbus, Électricité de France, Matra Marconi Space-France, Technicatome, Thomson-CSF) and LAAS-CNRS.