Performance Constraints for Onchip Optical Interconnects

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Abstract- This work aims at defining the marks that optoelectronic solutions will have to beat for replacing electric interconnects at chip level. We first simulate the electric response of future electrical interconnects considering the reduction of the CMOS feature size \( \lambda \) from 0.7 to 0.05 \( \mu \)m. We also consider the architectural evolution of chips to analyze the latency issues. We conclude that: 1) It does not seem necessary in the future chips to consider the integration of optical interconnects (OI) over distances shorter than 1000-2000 \( \lambda \), because the performance of electric interconnects is sufficient. 2) The penetration of OIs over distances longer than 10\( \lambda \) could be envisaged (on the sole basis of the performance limitation) provided that it will be possible to demonstrate new generations of (cheap and CMOS-compatible) low-threshold high-efficiency VCSELs and ultra-fast high-efficiency photodiodes. 3) The first possible application of onchip OIs is likely not for inter-block communication but for clock distribution as the energy constraints (imposed by the evolution of CMOS technology) are weaker and because the clock tree is an extremely long interconnect.

1. INTRODUCTION

The growth of the circuit complexity makes increasingly difficult the design of electrical interconnects (EI) in large chips. These issues have been predicted for (at least) two decades in several successive papers [1,2,3,4], and result from the increase of the chip operation frequency and from the reduction of dimensions. Taking these conclusions for granted, the fundamental question consists in appreciating whether the future limitations of intrachip communications might be solved by the “natural” evolution of existing electric technologies (as it is admitted by many people working in microelectronics), or whether they are more or less intrinsic and lead to some insuperable communication bottleneck in the next chip generations. If they are, optoelectronic interconnects (OI) have been suggested as an alternative solution [5,6,7,8, 9, 10, 11] because of the low crosstalk of optical signals, because of the large bandwidth represented by optical fibers in telecommunication, and because the power consumption is almost independent of the propagation distance (in optical fibers or wave guides).

When studying onchip interconnects, it is necessary to consider separately the clock distribution and inter-block communications. First, the clock distribution is not strictly speaking an onchip transmission, but the transmission of an external signal to the different isochronous blocks of the chip, involving a very long distribution tree. Second, the energy constraints of clock distribution are not so critical because the optical clock is generated by an external subsystem. Third, there is no latency issue as the clock is permanently transmitted. Thus, we defer the discussion of the possible use of OIs for distributing the clock to the last section of this work.

Logically, the first task (so far missing to our knowledge) to appreciate the possible role of optical interconnects consists in conducting communication simulations in the future CMOS chips, in order to clearly define the marks that optoelectronic solutions will have to beat. The evolution of the feature size of CMOS chips, and the evolution of the processor operation frequency are represented in Fig. 1. The extrapolation of the lines (Moore’s law) shows that, in ten years from now, processors will be clocked between 20 and 40 GHz and fabricated from the 0.05- or 0.07-\( \mu \)m process.

When discussing interconnect properties, it is essential to consider reduced units. In the following, we use:
- the feature size \( \lambda \) as length unit, so that interconnects with the same length approximately carry out the same functionality across the technologies. Of course, the reduction of \( \lambda \) will generate new extremely long interconnects (in \( \lambda \) unit) that do not exist today, for new architectures which also do not exist and that will have to be invented to use the huge number of transistors available in the next chip generations.
- the processor cycle \( T_C(\lambda) \) as time unit, for appreciating temporal communication issues in the future chips (bandwidth, latency…). The dependence of \( T_C \) versus \( \lambda \) in the future technologies is easily deduced from Fig. 1 by extrapolating the operation frequency curve \( F = I/T_C \) and the feature size curve over the next decade (extrapolations are represented by dotted lines).

We study in section 2 the evolution of the bandwidth, the latency and the power consumption of electric interconnects across the technologies from 0.35 to 0.05 \( \mu \)m. Optoelectronic interconnects are studied in section 3. We could not simulate the performance of the optoelectrical link across the technologies as we did for EIs, because of the difficulty to simulate the receiver stage (represented in Fig. 9) with SPICE
parameters, which is mostly an analogical cell, the SPICE parameters of which are still undefined for the future technologies. Thus, we only analyzed the performance of OIs in the current 0.18 \( \mu \)m process. In section 4, we compare the data of the previous sections, mostly to appreciate the marks that optoelectronic implementation will have to reach to beat electric solutions.

![Fig. 1: Evolution of the operation frequency and of the feature size of processor chips over 20 years and plausible evolution over 10 tens (dashed lines)](image)

**2. EVOLUTION OF ELECTRICAL INTERCONNECTS**

We need two models for studying the properties of electric interconnects: one model for the line, and another one for the CMOS transistors. Both models are used to simulate the line behavior with the analogical simulator SPICE.

- Today’s circuits include from 6 to 8 levels of metallic interconnects. We estimated the evolution of the line parameters \( w, h, t \) of medium-level interconnects from the observation of their reduction over two decades. This reduction is displayed in the left draft of Fig. 2. The symbols □, ◇, and △ represent the extrapolated and plausible values that we will use to calculate the electric properties of the future processes between 0.12 and 0.05 \( \mu \)m. We also consider the evolution of the materials (Cu replacing Al, change of the dielectric layers) to deduce the interconnect parameters \( R, L, \) and \( C \) used in simulations 12,13,14,15]. \( C \) is the capacitance between the line and the ground plane. Practically, it may be multiplied by a factor 2 (or even 3) when the interconnect is strongly coupled to other lines, as in the parallel bus configuration. The electrical interconnect is a distributed line modeled by a series of \( RLC \) quadrupoles [16].

For describing MOS transistors, it is necessary to choose an appropriate model that enables good representation of the MOS response and of its current emission. Complex models like MM9 or BSIM3 enable accurate representation of deep sub-micron MOS transistors but cannot be used to simulate future technologies, as they involve a large number of still undefined parameters. Fortunately, we do not need such sophistication, as our goal is not to accurately implement communications in a real architecture but to estimate the evolution of interconnect performance. Thus, for the technologies from 0.35 to 0.05 \( \mu \)m, we described the transistors in the framework of the simplified SPICE model-3 equations. We defined the model-3 parameters (for PMOS and NMOS transistors) from the physical parameters of future MOS transistors (VT, Tox, VDD, etc..) available in the semiconductor roadmap (SIA) [17], fitting the current-voltage characteristics with a fit precision of about 10%. We validated this approach by observing that the simulation results obtained with this method are close to those achieved with CADENCE for the 0.18 \( \mu \)m process.

![Fig. 2: Left: Evolution of line parameters across technologies. Right: interconnect cross section and identification of the physical parameters \( w, t, \) and \( h \).](image)
2.1. Bandwidth

The interconnect bandwidth is approximately defined as \( B=1/3t_E \), where \( t_E \) is the far-end risetime (FER), i.e., the time interval necessary to observe a signal transition from 10 to 90\% at the end of the line in the pulse regime. It is true that a single-piece interconnect (SPI) is bandwidth-limited depending on its aspect ratio \( S/L \) (\( S \): cross section, \( L \): length) [18]. However, there are two simple solutions to go around this limitation. The first one consists in enlarging the size of the transistors in the line driver to source a large current as shown by analogical simulations. The second one consists in including repeaters as displayed in Fig. 3. Simulations show that the far-end risetime of a line of length \( L \) including \( NR \) equidistant repeaters is very close to that of the section \( L/NR \) separately driven by a single inverter. Thus, the right parameter to characterize the FER is the inter-repeater distance measured in reduced units \( \lambda \) to directly compare the technologies. The FER dependence versus the inter-repeater distance is reported in Fig. 4 for the 0.18, 0.12, 0.1 and 0.05 \( \mu \)m processes. The right-most points represent a single-piece line because we consider the line driver as a repeater. The distance \( L=60,000 \lambda \) corresponds approximately to 1 cm in the 0.18-\( \mu \)m process. It must be stressed that the FER reported in Fig. 4 depends on the buffer size. We considered medium-size buffers. The FER could be twice longer when driving the line with very small buffers, but still shorter with larger buffers. Fig. 4 shows that the FER uniformly increases when sizing down the technology. However, there is no insuperable bandwidth limitation, as the solution consists in increasing the number of repeaters. When the repeater-repeater distance is smaller than \( LC=10^4 \lambda \), the FER is smaller that \( TC/3 \) (even in the finest technology), compatible with interconnects operating at the chip frequency. \( LC \) may be viewed as the inter-repeater separation, which enables to transmit data over any distance in the chip at the chip clock rate.

2.2. Latency

The latency of a single-piece interconnect versus the line length is represented in Fig. 5. We define the latency as the sum of the propagation time and the FER, representing the propagation from point A to point B in Fig. 3. Simulations show that the far-end risetime of a line of length \( L \) including \( NR \) equidistant repeaters is very close to that of the section \( L/NR \) separately driven by a single inverter. Thus, the right parameter to characterize the FER is the inter-repeater distance measured in reduced units \( \lambda \) to directly compare the technologies. The FER dependence versus the inter-repeater distance is reported in Fig. 4 for the 0.18, 0.12, 0.1 and 0.05 \( \mu \)m processes. Clearly, the reduction of the feature size induces a uniform increase of the latency at constant interconnect length (in \( \lambda \) unit). The figure shows that the latency remains typically shorter than \( TC/5 \) (\( TC \), clock cycle) as long as \( L<1000 \lambda \). Concretely, it means that two coupled functional blocks

![Fig. 3: Interconnect parameters](image-url)

![Fig. 4: Far-end risetime versus inter-repeater distance across several technologies](image-url)

![Fig. 5: Evolution of the latency across the technologies](image-url)
separated by a distance shorter than 1000λ have to sacrifice less than 20% of one clock cycle in communication and can still operate synchronously with at least a time interval as long as Tc/2 to process data.

The introduction of a few repeaters always reduces the latency of long interconnects. We report in Fig. 6 the reduction of the latency of a line L=5.6x10^4λ, across the technologies. Again, the right-most points correspond to a single-piece line. It turns out that the insertion of 4-5 repeaters typically divides the latency by a factor 2. Note the different behaviors of the FER (Fig. 4) and the latency (Fig. 6) when increasing the number of repeaters. The FER uniformly increases. Contrarily, the latency (which is FER plus the propagation time) first decreases and then increases due to the addition of the propagation in the inserted repeaters.

![Number of repeaters vs Propagation Time](image1)

**Fig. 6:** Latency versus the number of repeaters across the technologies. ■: 0.05 μm Cu/lowK, Tc=75-100 ps; ⊙: 0.1 μm Cu/lowK, Tc=150-200 ps; ▲: 0.012 μm Cu/lowK, Tc=300 ps.

### 2.3. Power consumption

The power dissipated in a SPL is plotted in Fig. 7 versus the interconnect length and for various processes ranging from 0.7 to 0.05 μm. The power dissipated in a repeated line can be easily deduced from these data as it is just the sum of the SPL power plus the power consumed by each additional repeater, which is represented the leftmost point of each curve in Fig. 7 (assuming that the repeaters are identical to the line driver).

The measurement of the power consumption in μW/GHz is not fully satisfactory to represent the power really consumed in the interconnects, as it is well known that the operation frequency of communications increases in the finest technologies. However, the operation frequencies of short and long interconnect are different. Typically, short interconnects (say for L<10^4λ) operate at the chip frequency F when long interconnects operate slower, down to F/3 or F/4. Thus, it is not simple to represent in a single diagram the frequency dependence and the distance dependence of the dissipated power. Simply multiply the power consumption reported Fig. 7 in by the interconnect operation frequency.

The consumption of short interconnects (say for L<100λ) approximately diminishes as the square of λ because it is dominated by the intrinsic capacitance of CMOS transistors. Contrarily, the consumption of long interconnects diminishes almost linearly. In the 0.18 μm process, we deduce that the power consumption is approximately (0.6-1) mW/mm/Gbit for interconnects extending from 0.2 to 5 mm.

![Power Consumption vs Line Length](image2)

**Fig. 7:** Power consumption of a single-piece interconnects across the technologies (SPICE simulation, CMOS model-3 of transistors). ■: 0.05 μm Cu/lowK, Tc=75-100 ps; ⊙: 0.07 μm Cu/lowK, Tc=150-200 ps; ▲: 0.012 μm Cu/lowK, Tc=300 ps; ▲: 0.18 μm Cu/lowK, Tc=660 ps; ▲: 0.25 μm Al/SiO2, Tc=1300 ps; ▲: 0.35 μm Al/AlSiO2, Tc=2000 ps; ⊙: 0.7 μm Al/AlSiO2.

### 3. OPTICAL INTERCONNECTS

The structure of an optoelectrical link is shown in Fig. 8. It comprises 3 stages: the emitter stage (left), the transmission medium and the receiver stage) that we describe in detail in the following.
Receiver stage: We followed the implementation proposed a few years ago by Ingels et al. [19] in the 0.35 process. The receiver implementation is represented in Fig. 9. It comprises a low-noise transimpedance amplifier (TA), several voltage amplifiers (A) and finally a decision circuit (C) to restore two unambiguous digital levels from the noisy photocurrent. The decision circuit is nothing but a voltage comparator, which compares the output of the transimpedance amplifier to a reference threshold $V_{th}$. The rate of erroneous bits (BER) generated by the decision circuit critically depends on the input signal to noise ratio (SNR), i.e., on the ratio of the photocurrent divided by the equivalent input noise of the transimpedance amplifier. Practically [20], an input photocurrent larger than 1 $\mu$A is sufficient (at 1 Gbit/s) to warrant a SNR larger than 20, and a BER as low as $10^{-20}$ with most photodiode-TA configurations.

The receiver consumption represents the energy necessary to convert the input current $I_{ph}$ generated by the photodetector into electric logical levels. The minimization of the receiver consumption forces to adjust the size of the transistors versus the photocurrent.

Emitter-receiver transmission medium: The coupling of the VCSEL emission to a fiber or to an optical guide induces energy losses. For our analysis, we may reasonably estimate the transmission factor $\eta_\text{C}$ from the emitter to the photodetector to be of the order of 60-70 %, independently of the various technologies that can be involved.

Emitter stage: The energy is dissipated in the driver stage to generate a current exceeding the threshold current $I_{TH}$ that triggers the laser emission. We consider VCSEL diodes. This energy critically depends on the threshold current and on the quantum efficiency of the VCSEL. At the moment, it is of the order of (0.5-2) mA for commercial VCSELs [21] and as low as 100 $\mu$A with laboratory components [22-23]. The power dissipated in the driver reads (Eq. 1):
\[ P_E(I_{ph}) = V_S \left( I_{ss} + \frac{I_{ph}}{2\eta_D\eta_E\eta_C} \right) \]

where \( I_{ss} \leq I_{th} \) is the steady state current in the emitter, \( I_{ph} \) the photodetector current, \( \eta_E , \eta_D \) the quantum efficiencies of the emitter and of the detector respectively, and \( \eta_C \) the transmission factor from the emitter to the photodetector.

The total power \( P \) consumed by the optical interconnect is the sum of the power \( P_E \) consumed by the emitter and \( P_R \) consumed by the receiver. It reads:

\[ P(I_{ph}) = P_E(I_{ph}) + P_R(I_{ph}) \]

Fig. 10 displays the increase of the consumption versus \( I_{ph} \) considering that the receiver and the emission laser have quantum efficiencies close to the optimum value, close to 0.8.

The shortest propagation delay through the detection stage represented in Fig. 9 was approximately 210 ps.

4. COMPARISON OF ELECTRICAL AND OPTICAL INTERCONNECTS

4.1. Bandwidth limitation

Fig. 4 shows that there will not be insurmountable bandwidth issues in the future chips. The insertion of repeaters extends the bandwidth if necessary. With repeaters approximately distant of \( L_c = 10^4 \lambda \) (for the processes between 0.18 and 0.05 \( \mu \)m), it might be possible to transmit data over any distance at the chip clock rate, although it is known that in most architectures, long distance communications are (so far) clocked at typically 30-50% of the chip frequency. However, an issue might appear for architectures requiring tens of thousands of long interconnects (see the discussion in paragraph 5).

4.2. Power consumption

It is very easy from Fig. 7 to compare the power consumed by electrical and by optical interconnects in the present state of the competition, with all electronic circuits based on the 0.18 \( \mu \)m process. The consumption of the OI is represented by the upper horizontal grey bar in the figure. The intersection of this line with the curve representing the consumption of the 0.18-\( \mu \)m process defines a critical length \( L_c \) (that we designate as the penetration length in the following) of the order of \( (1-2) \times 10^4 \lambda \), i.e., 3-4 mm. Therefore, the advantage of OIs, regarding the energy consumption, becomes really strong when considering propagation distances of the order of (5-10) mm, i.e., for long intrachip communication channels.

Perhaps, it is more important to appreciate the constraints imposed by the reduction of the energy consumption of EIs. If we wish to maintain the penetration of OIs for lengths longer than \( L = (1-2) \times 10^4 \lambda \) in the future 0.05 \( \mu \)m process, Fig. 7 shows that it will be necessary to divide the present consumption by about 50. If we want to increase the potential penetration of optics down to \( 10^3 \lambda \), the consumption would have to be reduced down to 10 \( \mu \)W, correspondingly to a reduction of about 200. It results that the OI driver consumption ought to be of the order of 5 \( \mu \)W (assuming reasonably that 50% of the total energy is dissipated in the driver and 50% in the receiver), requiring the development of new VCSEL generations with threshold currents as small as a few \( \mu \)Amps and high quantum efficiency \( \eta_E \).
Fig. 11: Power consumption with “degraded” components such that $\eta_E = 0.15$ and $\eta_D = 0.15$

4.3. Latency issue

Fig. 5 shows that the latency of a SPI remains lower than $0.2 T_C$ as long as the interconnect length is shorter than $L_C = 1000 \lambda$. Additionally, Fig. 6 shows that the insertion of 4-5 repeaters always reduces this time, typically by a factor 2. Thus, the reduction of dimensions will not call into question the performance of most interconnects. Nevertheless, the latency will significantly increase in the finest technologies (i.e., in the 0.05 $\mu$m process) for the longest links, to reach several tens of clock cycles when $L > 10^5 \lambda$.

If the high latency penalizes the performance, OIs might represent an appealing alternative, as the latency of a 2-3 cm OI could likely be maintained around 3-5 chip cycles in the future technologies. For instance, in the 0.05 $\mu$m process operating around 10 GHz, the sole propagation over 2 cm lasts 100 ps (i.e., 2 clock cycles). The latency of the receiver, which is about 200 ps in the 0.18 $\mu$m, could be likely between 50 and 100 ps in the future, corresponding to a global latency of about 4 cycles.

5. LONG INTERCONNECTS IN FUTURE ARCHITECTURES

Regarding latency, and the interest of replacing long electrical links with OIs, it is crucial to appreciate how the high latency of long interconnects will penalize the performance of the future architectures as they have no functional equivalence in today’s chips. The answer clearly depends on the evolution of chip architectures (and particularly processors) that we very briefly survey in this section. We review the plausible evolution for general-purpose processors, onchip SMP, DSP and FPGA.

5.1. Monoprocessor

The concepts of RISC processors have been extended to all today’s processors, generalizing the pipeline operation mode: Each instruction is read in the memory, decoded and operands are read in the registers, then the requested operation is executed in the arithmetic unit and finally, the result is written in the registers or in the memory. Thus, each instruction passes through the different pipeline stages. The four stages we just described correspond to a simple processor. Each stage can be still split to improve the pipeline throughput. Current processors have from 10 to 20 stages, as the Pentium 4. The information flow is (mostly) unidirectional. All pipeline stages are adjacent (or very close) as demonstrated by all microphotographs of processor chips [24], and one does not expect long interconnects issues here.

The processor pipeline works smoothly and efficiently if its input stage can (typically) read one instruction per cycle. But this would require an access time to the memory of 1 processor cycle that is completely impossible. In fact, the processor cycle has decreased much faster than the intrinsic memory access latency (MAL), which therefore represents an increasing number of processor cycles. It is today of the order of 80-100 cycles. Thus, the evolution of PCs and multiprocessor machines has consisted primarily in hiding the MAL with software or hardware solutions because it has been impossible to change the memory technology. Hardware solutions comprise:

- Caches between the processor and the main memory to hide the MAL by limiting the number of accesses to the memory.
- Several functional units to implement additional mechanisms, to avoid as much as possible the pipeline stall, as out of order execution of instructions, branch prediction techniques (successful 95% of the time), speculative execution, and prefetching.

Additionally, all today’s processors are superscalar. They try to execute several instructions simultaneously, (typically from 4 to 8) that still increases the memory throughput need.

The chip layout reflects this evolution. The mechanisms we just described consume many transistors, typically between 10 and 20 millions in the latest processors...
connected network of processors might need numerous multiprocessors are also envisaged [31]. A fully inter-

favorable to the integration of OIs). 2D meshes or tori associated in different communication networks: one or several shared busses (that might generate long links that could propagate for several tens of nanoseconds). The processor cores and memories can be shared data in several caches generates an additional preservation of the coherence of the multiple copies of the same data. The general issues of the memory hierarchy. The last level cache (L3) with several megabytes has an access time of a few processor cycles, whereas the access time of the memory [28, 29]. The 174 millions of transistors of the IBM Power4 chip is used to integrate 2 processor cores and 1.66 Mbyte of memory [28, 29].

The number of long interconnects (say typically longer than 1 cm) reduces to a few buses (see for instance figure 22 in [29]). The cache memory is in fact a hierarchy. Today, it is mainly composed of 3 cache levels (L1, L2, L3), because it is impossible to build a cache that would be simultaneously large and fast! L1 has a size of a few kbytes, to keep the access time equal to 1 processor cycle (PC). L2 has a size of a few hundreds of kbytes with an access time of 5-10 PCs, and L3 with several megabytes has an access time of a few tens of PCs. Clearly, L3 has the largest distance to the processor core, but the interconnect latency is not critical, as it represents a fraction of the intrinsic cache latency.

In this context, it does not seem that, in the monoprocessors, the huge increase of the number of transistors and the architectural evolutions generate insuperable long-interconnect issues.

5.2. Onchip symmetric multiprocessors

The integration of several processor cores in a single chip essentially transfers at the chip level the known issues of multiprocessors. At the moment, single-chip SMP studies are limited to 8 processors that will share the last cache level [30]. The integration does not change the general issues of the memory hierarchy. The preservation of the coherence of the multiple copies of shared data in several caches generates an additional traffic. The processor cores and memories can be associated in different communication networks: one or several shared busses (that might generate long links) are envisaged [31]. A fully interconnected network of processors might need numerous long interconnects but it is not realistically considered.

5.3. DSP

Digital Signal Processors are specific chips used in all applications related to signal processing, in particular in multimedia applications. Signal processing is on-the-fly processing of a continuous data flow, generally through a multistage pipeline (with no feedback most of the time) that involves very few long interconnects because it is generally composed of adjacent functional blocks.

5.4. FPGA

FPGA are composed of arrays of programmable logic blocks. The main interest of FPGA is their reconfiguration or programmability features. However, besides this advantage, the communication issues are not very different in essence from those previously described. If the FPGA is used in pipeline architecture, there will be few long interconnects. If the FPGA is used to customize a monochrome or multiprocessor architecture, blocks with latency-sensitive links will be nearby.

6. CONCLUSION

The simulation of the electric communications in the future CMOS processes enables to estimate the performance of OIs when they will be integrated in the future chips. This evolution partly comes from the simple fact that the number of available transistors (several billions of transistors on a single chip around Y2010 [17]) increases much faster than the capability of architects to design new processor cores [25, 26]. The simplest and cheapest solutions (at least in a first step) to use the transistor budget and to increase the performance consists in increasing the size of caches or in integrating several identical processor cores. For instance, in the latest Intel Itanium2, 80% of transistors (over 221 millions) are used by 3.3 Mbyte of caches [27]. The 174 millions of transistors of the IBM Power4 are used to integrate 2 processor cores and 1.66 Mbyte of memory [28, 29].

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- The first possible application of onchip OIs is likely not for inter-block communication but for clock distribution. The replacement of electric interconnects by optical links for clock distribution seems less complicated than the massive replacement of interblock communication links that we studied in the previous sections. This replacement might be an important evolution to reduce the clock distribution skew and to ensure the isochronous operation of the chip when the operation frequency will be near 10-20 GHz. It will be less complex because the clock source (i.e., the light emitter) can be external to the chip, removing a fraction of the consumption energy constraints and also the difficult problem of integrating III-V optoelectronic emitters on top of Si CMOS circuits. A full CMOS-compatible process including Si-photodetectors is feasible even if the quantum efficiency of CMOS-compatible Silicon photodetectors is small [32,33,34,35].

Finally, we must stress that the competition between OIs and EI's does not reduce to the sole bandwidth, latency and energy-consumption issues that we considered in this work. EI's are embedded in a more or less dense network, with communication crosstalks resulting from the capacitive coupling of close lines. This effect, especially important for interblock busses, generates the crosstalk noise. OIs could be attractive here because there is no intrinsic coupling between optical interconnect lines, or between an optical line and an electrical line.

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REFERENCES


