Fundamental Performance Limits and Scaling of a CMOS Passive Double-Balanced Mixer

Krenar Komoni1, 2, Sameer Sonkusale3, Geoff Dawe2
1Electrical and Computer Engineering Department, Tufts University, Medford, MA 02155
2BitWave Semiconductor, Incorporated. Lowell, MA 01851
E-Mail: {kkomoni, geoff}@bitwave.com, sameer@ece.tufts.edu

Abstract—In this paper, fundamental performance limits and scaling of a double-balanced passive mixer are examined. Analysis of the passive double-balanced mixer will show how its performance metrics are directly affected by the down-scaling of the transistor gate length, L G. We analyze the performance in terms of conversion gain (G C), 1-dB compression point (P 1-dB) which we derive, and SSB Noise Figure (NF). We will show that as CMOS process technology evolves, the double-balanced passive mixer architecture will become more favorable and yield improved performance. This is verified through simulation and modeling results for mixers designed in CMOS 350nm to 32nm technology. We introduce a mixer’s figure-of-merit (FOM MIXER) to compare performance with technology scaling. Circuit designers and System architects can use this paper to find a suitable process technology that will meet their specifications.

I. INTRODUCTION

In the early 90s, as the bipolar technology was threatened, there was a major push towards replacing bipolar transistors with CMOS transistors, especially in the analog components of wireless transceivers. The motivations behind this shift were, creating highly integrated transceivers with significant power savings as shown in [1] and meeting the industry trend on reducing the overall system pin requirements as the device size scales down. Today, after many years since the shift has occurred, new questions and challenges have surfaced: how far can CMOS technology take us? Furthermore, will wireless transceiver components reach their fundamental operational performance limits as the CMOS process technology scales down [3]?

The mixer is one of the most crucial components in a wireless transceiver. In CMOS technology, the two mixer architectures that are popular and most commonly used are: the active double-balanced mixer, or the Gilbert mixer [4]; and the passive double-balanced mixer, or the FET-Quad mixer [5]. The comparison of their performance in 0.35um CMOS is shown in [6]. Passive mixers have the significant advantages of not requiring dc bias current, not dissipating standby power, having high-linearity, and commutating the signal in the voltage domain. Thus, they are well suited for applications requiring low flicker noise and low power consumption [7]. However, drawbacks of high noise figure, limited bandwidth, and high conversion loss will significantly improve due to the device size scaling down.

The following analysis will explore the fundamental limits of voltage conversion gain, 1-dB compression point, IIP3, and noise figure of the passive mixer based on the fundamental CMOS process technology parameters as the device size scales down. The analysis, equations, and model results are a simplified approximation of the passive double-balanced mixer. Finally, the new figure-of-merit (FOM) is introduced in relation to the fundamental parameters of the technology.

II. PASSIVE DOUBLE-BALANCED MIXER (FET-QUAD)

The passive double-balanced mixer, also known as the FET-Quad mixer, is an old structural concept that has been introduced prior to the forthcoming of CMOS technology in the RFIC industry [8]. A double-balanced passive mixer using CMOS technology is shown in Fig. 1. The double-balanced structure helps with LO-IF and RF-IF isolations. The RF and the LO ports use baluns to generate differential signals. In this model the baluns are assumed to be ideal.

The FET-Quad mixer is mainly made of four switches that turn ON and OFF, generating the mixing process between the RF and LO ports. The IF signal is taken from the source; the RF signal is fed to the drain; and the LO signal is fed to the gate of each transistor. The LO signal modulates the channel resistance (conductance) and mixes the RF and LO frequency signals in the voltage domain. For an optimum IF signal transfer, the LO signal should be applied along with a dc gate bias around the NMOS
threshold voltage ($V_{th}$) [6]. As a result of this process the remaining frequency components are: $\omega_{RF} - \omega_{LO}$, $\omega_{RF} + \omega_{LO}$, and other harmonics which are multiples of RF and LO frequencies, $m\omega_{RF} \pm n\omega_{LO}$. A band-pass filter can be used to filter out the higher order harmonics giving us a fundamental mixing component of $\omega_{RF} - \omega_{LO}$ or $\omega_{RF} + \omega_{LO}$.

III. ANALYSIS OF THE FET-QUAD MIXER

The analysis of the mixer will be broken down into two parts. First, a model of a single-transistor passive unbalanced mixer will be introduced. Later, this model will facilitate modeling and analysis of a passive double-balanced mixer. When operating a mixer, it is ideal to have a local oscillator (LO) that generates a square wave signal. This minimizes the transition time between the ON and OFF states of the transistor. It is during the transition (triode region) period that most of the noise is inflicted from the RF to the IF port and when intermodulation distortion occurs. Utilization of a square LO wave also results in conversion gain loss. We therefore plan to compare mixer performance utilizing the following parameters: voltage conversion gain, IIP3, 1-dB compression point, and noise figure. In the end we will introduce a novel figure-of-merit (FOM) which combines all the above.

A. Voltage Conversion Gain

In the following analysis of the voltage conversion gain, LO driver is assumed to generate perfect square waves. The LO signal is expressed in (1) and shown in Fig. 2a. This assumption can be made effortlessly and carried out across all the analyses, because the focus of this paper is on the fundamental limits of the passive mixer.

$$v_{LO,\text{square}} = \frac{1}{2} + \frac{1}{\pi} \left[ \sin(\omega_{LO}t) + \frac{\sin(3\omega_{LO}t)}{3} + \frac{\sin(5\omega_{LO}t)}{5} + \ldots \right]$$  \hspace{1cm} (1)

After multiplying the RF signal $\cos(\omega_{RF}t)$ with the LO signal in (1), the voltage conversion gain for an ideal passive mixer using one transistor becomes: $20\log_{10}(1/\pi) = -9.943$. In order to reach the ideal value of -9.943 dB, the device that performs the multiplication should not introduce any undesired output frequencies due to its nonlinear characteristics or its high frequency limitations.

The analysis of a single-transistor passive mixer voltage conversion gain is divided into two states: 1) the mixer is viewed as an LTI system where the transistors are static (not switching) and 2) the mixer is viewed as an LPTV system [10] where transistors are dynamic (switching). The combination of these two states is used to generate the final conversion gain value.

First, let us consider a mixer that is constructed with a single switch. The model of the switch is shown in Fig. 2b. When the switch is on, impedance $R_{ON}$ (2) is the combination of the source resistance $R_s$, drain resistance $R_d$, on-resistance $r_{ds}$, and the transistor capacitances (Fig. 3). We will ignore $R_s$ and $R_d$ assuming they are much smaller than the on-resistance $r_{ds}$. When the switch is off, the impedance $Z_{OFF}$ (3) is assumed to be dominated by the linear gate-drain and gate-source capacitances. The nonlinear drain-bulk capacitance and source-bulk capacitance can be ignored assuming a low frequency LO case. This assumption is valid for our discussion as we are interested in studying the impact of technology scaling on mixer performance.

$$R_{ON} = r_{ds} = \frac{L_s}{\mu C_{ds} W \left( (V_g - g_c v_{gs}) - V_a - V_d \right)}$$ \hspace{1cm} (2)

$$Z_{OFF} = j \left( j \omega_{LO} \left( C_{Gd}(V_g,0) \| C_{Gb}(V_g,0) \right) \right)$$ \hspace{1cm} (3)

During the first state, the voltage conversion gain can be calculated by looking at the mixer as a simple LTI system. When the switch is closed in Fig. 2b, the conversion gain becomes:

$$g_c = \frac{Z_L}{|Z_L + R_{ON}Z_{OFF}|}$$ \hspace{1cm} (4)

And, when the switch is open the conversion gain of the LTI system is assumed to be very close to zero:

$$g_c = \frac{Z_L}{Z_L + Z_{OFF}}$$ \hspace{1cm} (5)

In the second state, when the transistor starts switching through the ideal square wave that is generated by the LO drive, the system becomes a LPTV system with conversion gain that reduces to (6). More detailed derivations can be found in [10].

$$g_c = \frac{1}{\pi} \left( \frac{Z_L}{Z_L + R_{ON} Z_{OFF}} \right)$$ \hspace{1cm} (6)
For the analysis of the FET-Quad mixer shown in Fig. 1, a similar model can also be applied for each transistor. An overall transistor level model for the double-balanced mixer is introduced and presented in Fig. 4. The analysis of the model is completed by adding the output differentially at the IF port. Hence, obtaining a final conversion gain equation that is equal to (7), with the assumption that the capacitances in the off and on state are linear.

\[
G_c = 20 \log_{10} \left( \frac{2}{\pi} \frac{Z_L}{Z_L + R_{ON}} \parallel Z_{OFF} \right) - 2 \left( \frac{Z_L}{Z_L + Z_{OFF}} \right)
\]

Equation (7) shows how the value of the transistor on-resistance $R_{ON}$ is clearly the limiting factor in obtaining a conversion gain that is as close to the ideal, $2/\pi$. The on-resistance equation for the NMOS switch in a passive mixer can be expressed in the following form:

\[
\mu \left( \frac{W}{L} \right) \left( V_{DS} - V_{TH} \right)
\]

Hence, channel length $L$, mobility $\mu$, and oxide capacitance $C_{ox}$, of the process play a major role in the value of the on-resistance. As the channel length gets smaller, the $R_{ON}$ also gets smaller, thus improving the conversion gain of the passive mixer. The tendency is to increase the width ($W$) in order to reduce the value of $R_{ON}$, however, the intrinsic capacitances increase proportionally to $W$, thus reducing the value of $Z_{OFF}$ and creating a frequency limitation in the mixer [6]. A helpful graph for different gate lengths can be found in [15]. The other factor contributing to negative conversion gain is the appearance of image and harmonic frequencies at the IF port, which are neglected in this paper.

B. 1-dB Compression Point and IIP3

When using NMOS transistors as switches, the maximum output large signal voltage that can be achieved is equal to $V_{LO,max} - V_{th}$. This phenomenon causes the passive mixer to have a limitation at its 1-dB compression point and third-order intercept point (IIP3). In this paper, the IIP3 is treated as being 9.635 dB above the 1-dB compression point. Due to the assumptions made above, the second order products are cancelled. Transmission gates and boot strapping techniques can be used to improve the linearity of the CMOS passive mixer [13] with some limitations in area and performance. Equation (2) shows that the on-resistance is directly proportional to the input voltage, and as the input voltage $g \cdot v_{g}$ approaches $V_{g} - V_{th}$ the on-resistance increases. Due to the non-linearity of the on-resistance, the output signal $v_{g}$ starts to compress, and it eventually hits the 1-dB compression point. Using polynomial fitting techniques the approximation of the output voltage in terms of $c_1$, $c_2$, $c_3$, and $c_4$ coefficients can be achieved [14]. We derived the expression in (9) by expressing $v_{g} = g \cdot v_{g}$ in a power series form and solved for the coefficients. From the coefficients shown in (8) and (9), the 1-dB compression can be computed and is shown in (10).

\[
v_{g} = c_0 + c_1 v_{g} + c_2 v_{g}^2 + c_3 v_{g}^3 + \cdots
\]

\[
Z_{L} \left( \frac{L_s}{\mu C_{ox} W (V_{g} - V_{th} - V_{a})} \right) \left( Z_{L} + \frac{Z_{OFF}}{Z_{OFF}} \right)
\]

Assuming that the LO drive is operated at the $V_{th}$ of the technology, Fig. 5 shows how 1-dB compression point decreases as the channel length scales down.

C. Noise Figure

With the forward progression of CMOS technology, the minimum noise figure of the FET device keeps improving [15] (Fig. 5), mainly due to the $f_t$ of the device. In this analysis, the flicker and white noise that occur due to the ON and OFF overlaps of a sinusoidal LO waveforms [6] are ignored. The sharp transitions lead to having either M1 or M2 conductance ($g_{m}$) introduce noise in the passive double-balanced mixer. The passive mixer’s output voltage noise spectral density is equal to $v_{n}^2 = 8kT/l_{on}$ [7]. The final noise figure (11) includes the conversion gain $G_c$, where F is equal to the noise factor generated by the mixer itself.

\[
F = \frac{1}{G_c^2} + \frac{F_{MIN}}{G_c^2 \cdot kT/l_{on}} = \frac{1}{G_c^2} + \frac{8kT/l_{on}}{G_c^2 \cdot kT/l_{on}}
\]

\[
\Rightarrow SSB NF = 10 \log_{10} \left( \frac{1}{G_c^2} + \frac{2}{G_c^2 \cdot kT/l_{on}} \right)
\]

IV. MEASUREMENT AND SIMULATION RESULTS

The simulated results for conversion gain, 1-dB compression point, and NF shown in Fig. 5 were obtained using Cadence Spectre-RF at 130nm and 65nm technologies with accurate high frequency transistor models [9]. Matlab FET-Quad model results are also shown in Fig. 5 and are compared with metrics from other references and with measured results validating the model.
We also characterize our custom mixer in 130nm technology against the model, see Fig. 5. Our custom mixer is shown in Fig. 6, and it has been tested with an LO frequency of 900MHz and an RF of 905MHz, resulting to an intermediate frequency (IF) output at 5MHz. The LO power was set to +7dBm, and the conversion gain was measured at -4.7 dBm, and 1-dB compression point occurred at 0.4 dBm. The LO and the RF port contain baluns to generate differential signals, whereas the IF port does not contain a balun. Both RF and LO ports are matched to 50Ω impedances.

We now introduce a figure of merit that will determine the performance of passive or active mixers. The \( FOM \) is similar to the one in [19] except that \( V_{dd} \) is neglected, power consumption is defined differently, and \( FOM \) is expressed in \( \text{dBm} \) scale.

\[
FOM = G_r - SSB NF + P_\text{1-dB} - P_\text{CONSUMED} \quad (12)
\]

Even though the passive mixer does not consume any dc power, the LO power that is used to drive the passive mixer is included in (12), where \( P_\text{CONSUMED} = V_{dd}/2R + P_{LO} \). The \( FOM \) is plotted as a function of technology in Fig. 5.

V. CONCLUSIONS

In this paper the fundamental performance limits of a double-balanced passive (FET-Quad) mixer were presented. As the CMOS process technology evolves and the gate length of the MOSFET device decreases, the performance parameters of the FET-Quad mixer reach their ideal fundamental limits. Our model has been validated using theory, simulation, and measurement. In the near future, passive mixers will be preferred by many circuit designers for meeting system specifications and improving performance. Our model provides the necessary tools to compare different technologies for mixer performance.

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