Improved Cascaded Delta-Sigma Architecture with High Signal to Noise Ratio and Reduced Distortion

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Abstract—An architecture of cascaded delta-sigma modulator is presented. It attains a significant improvement in achievable SNR, dynamic range and has the additional advantage of reduced sensitivity to switch and op-amp nonlinearities. The design consists of approximating quantizer-gain by functional simulation of the modulator and then keeping this value in view while conceiving digital filters. Digital filters designed this way are more efficient in cancelling quantization error and provide better results. This architecture can be used at low oversampling ratios for wideband applications, as well as for high-resolution audio applications.

I. INTRODUCTION

Traditionally, delta-sigma converters have been employed in low bandwidth applications such as digital telephony and digital audio [1]. These applications rely on high oversampling ratio (OSR) to achieve the desired SNR and linear performance. However, during recent years, due to continuous scaling of CMOS technologies, delta-sigma conversion is becoming attractive for use in wideband applications such as in RF-front ends. At low values of OSR required for such applications, it is not possible to obtain high SNR in a single-quantizer modulator simply by raising the order of the loop filter, since stability considerations limit the permissible input signal amplitude for higher-order loops. The SNR can still be increased by using more bits in the internal quantizer, but this requires a flash ADC and also means to insure the in-band linearity of the internal DAC [2]. As a result, the complexity of the quantizer grows exponentially with the number of bits used in it. Hence, this number can seldom be higher than 4 or 5 bits.

A different strategy, which relies on the cancellation rather than the filtering of the quantization noise, is to use a multi-stage or MASH (for Multi-stAge noise-Shaping) structure for the modulator. It is also called Cascade structure.

In this paper, a fourth-order cascaded delta-sigma topology with improved SNR, dynamic range and reduced sensitivity to integrator nonlinearities is described. The technique is effective for any oversampling ratio.

II. TRADITIONAL CASCADE ARCHITECTURE

In a cascade structure, each stage is realized by a delta-sigma modulator. The quantization error of one stage is fed as an input to the next stage. The output of the next stage is then an approximation of this quantization error. The digital filters $H_1(z),...,H_n(z)$ are designed so as to cancel the quantization error of all but the last stage in the output and to attenuate the last stage quantization noise by an order equal to the order of the modulator.

In order to concisely differentiate between the various cascade combinations, cascaded modulator topologies are referred to by a sequence of numbers corresponding to the order of the differential noise shaping provided by each stage in the cascade. The first number corresponds to the first stage, the second to the second stage, and so on.

We use necessarily a $2^{nd}$ order delta-sigma modulator as the first-stage of MASH Modulators, because it achieves stable, high-order performance without the strict matching requirements that characterize cascades of first-order stages [3]. Furthermore, the use of second-order noise-shaping in the first stage of a cascade avoids the potential presence of discrete noise tones in the output of the overall cascade.

Fig. 1 shows the traditional cascade 2-2 architecture of delta-sigma modulators, which is well known for its guaranteed stability for the full input range. A related cascade 2-1-1 architecture has been reported in [4]. Unfortunately, this traditional architecture suffers from distortion due to sensitivity to opamp nonlinearities [5].

III. ENHANCEMENTS ON THE TRADITIONAL ARCHITECTURE

A single stage low-distortion delta-sigma converter has been proposed in [5]. The performance requirement of the integrators is significantly relaxed in this topology by removing the input signal out of them, so that they only have to process quantization noise. It has reduced sensitivity to opamp nonlinearities and thus exhibits lower distortion than traditional single-stage topologies.

A cascade architecture employing these low-distortion single-stage converters is presented in [6]. This is a two stage
cascade structure in which both stages are realised by Silva’s structures [5]. An enhancement on Gothenberg’s topology [6] is proposed in [7], which achieves better results by using optimized coefficients.

IV. PROPOSED TOPOLOGY

To achieve an improvement over attainable SNR of cascaded delta-sigma modulator, we present a modified cascaded architecture shown in Fig. 2. Like Gothenberg’s structure [6], both stages stages are realized with low-distortion, feed-forward Silva’s structures [5]. This improves SNR in the desired baseband, as the first-stage quantization error is not affected by the second-stage integrator nonlinearities [6].

Since $e(n) = out(n) - G \cdot in(n)$, where out is quantizer output, in is quantizer input and $G$ is quantizer gain, the average power of $e$ can be written as,

$$
\sigma_e^2 = \frac{1}{N} \sum_{n=0}^{N} (out(n) - G \cdot in(n))^2
$$

This is minimized for,

$$
G = \frac{1}{N} \sum_{n=0}^{N} in(n) \cdot out(n)
$$

When a system containing a binary quantizer is replaced by its linear model, the estimate of the quantizer gain $G$ is found from numerical simulation [8]. Since, we are using binary quantizers in our structure, we find the quantizer gain $G1$ of the first-stage quantizer using simulation data and Eqn. 3. The evoloution of $G1$ with input signal amplitude is shown in Fig. 4.

A. Quantizer Linear Model and Quantizer Gain Calculation

The linear model of the quantizer, shown in Fig. 3 is very important in our design of cascaded $\Delta\Sigma$ modulator structure. This model approximates the non-linear quantizer by a gain $G$ called ‘quantizer gain’ in series with an additive gaussian noise source. This approximation, which is valid when the quantization step is small as compared to the signal amplitude, is also used for low-resolution quantizers where it is not verified.

$$
\sigma_e^2 = \frac{1}{N} \sum_{n=0}^{N} e(n)^2
$$

B. Digital Filters’ Designing

Digital Filters i.e $H1$ and $H2$, are designed to achieve two major objectives,

- To cancel the effect of first-stage quantization noise in the output
- To provide fourth-order noise shaping to the second-stage quantization noise in the output

From Fig. 2, using linear model of the quantizer presented in Section. IV-A, the output of first-stage modulator is,

$$
Y1 = \frac{G1}{D1(z^{-1})} \cdot X + \frac{(1 - z^{-1})^2}{D1(z^{-1})} \cdot E1
$$

where $G1$ is the first-stage quantizer gain and,

$$
D1(z^{-1}) = 1 - (2 - 2G1)z^{-1} + (1 - G1)z^{-2}
$$
and similarly the output of second-stage modulator is,
\[ Y_2 = -\frac{G_2}{D_2(z^{-1})} E_1 + \frac{(1 - z^{-1})^2}{D_2(z^{-1})} E_2 \]
where \( E_1 \) is the quantization noise of first-stage, \( G_2 \) is the quantizer gain of second-stage, and,
\[ D_2(z^{-1}) = 1 - (2 - 2G_2)z^{-1} + (1 - G_2)z^{-2} \]

1) Second-Stage Quantizer Gain \( G_2 \): The second-stage quantizer gain \( G_2 \) has insignificant effect on the final output, since the second-stage processes only the quantization error of first stage. So we assume its classical value i.e 1 which results in a simple filter \( H_2 \). Putting this value in Eq. 6, we get a nice expression for \( Y_2 \),
\[ Y_2 = -E_1 + (1 - z^{-1})^2 E_2 \]  

2) First-Stage Quantizer Gain \( G_1 \): Assumption of a value for \( G_1 \) plays a major role in determination of digital filters. It is at this point that our structure differs from the classical ones:
- In the classical structures, we assume \( G_1 \) to be equal to 1, which is not in accordance with simulation data presented in Fig. 4. Nevertheless, this assumption results in a nice expression for \( Y_1 \),
\[ Y_1 = X + (1 - z^{-1})^2 E_1 \]
Now solving the equation,
\[ Y_1 \cdot H_1 + Y_2 \cdot H_2 = X + (1 - z^{-1})^4 E_2 \]
leads to very simple digital filters,
\[ H_1 = 1 \]
and,
\[ H_2 = (1 - z^{-1})^2 \]
- For our structure, we do not assume the value of \( G_1 \) to be equal to 1. As shown in Fig. 4, the value of \( G_1 \) varies between 0.75 and 0.1. We have tested the system performance at multiple values of \( G_1 \) in this range. As we decrease the value of \( G_1 \), the dynamic range increases but the SNR decreases. We find that taking \( G_1 \) to be equal to 0.5 gives the best compromise between dynamic range and SNR as shown in Fig. 5.
Therefore, the proposed structure consists of assuming \( G_1 \) to be equal to 0.5. With this value of \( G_1 \), we find the first-stage output as,
\[ Y_1 = \frac{0.5}{1 - z^{-1} + 0.5z^{-2}} X + \frac{(1 - z^{-1})^2}{1 - z^{-1} + 0.5z^{-2}} E_1 \]
Solution of the set of Eqns. 8, 10 and 13 now gives us the digital filters to be,
\[ H_1 = 1 - z^{-1} + 0.5z^{-2} \]  
and,
\[ H_2 = (1 - z^{-1})^2 \]  

So, two different assumptions for \( G_1 \) result in two different values for \( H_1 \). \( H_2 \) remains constant.
Our proposed topology consists of making systematic assumption for \( G_1 \) based on numerical simulation, and then design the digital filters based on this value. Using these proper values of quantizer gains and digital filters results in more effective cancellation of quantization noise and thus better SNR is achieved.
We also propose a cascade 2-1-1 architecture, shown in Fig. 4.

Fig. 5. Effect of quantizer gain \( G_1 \) on SNR curve

![Fig. 5. Effect of quantizer gain \( G_1 \) on SNR curve](image)

It is designed on the same principles as outlined for cascade 2-2 architecture above. This architecture attains superior performance than cascade 2-2 architecture in terms of quantization noise suppression. All three stages are realized with low-distortion, feed-forward Silva’s structures [5].

The quantizer gains \( G_1 \), \( G_2 \) and \( G_3 \) that are used for this architecture are 0.5, 1 and 1 respectively. These optimized
values of quantizer gains result in following digital filters:

\[ H_1 = 1 - z^{-1} + 0.5z^{-2} \]  \hspace{1cm} (16)

and,

\[ H_2 = (1 - z^{-1})^2 \]  \hspace{1cm} (17)

and

\[ H_3 = (1 - z^{-1})^3 \]  \hspace{1cm} (18)

The same methodology can be used to design any cascade structure.

V. SIMULATION RESULTS

In the simulations, we have compared four types of cascaded delta-sigma architectures:

1) The Gothenberg’s cascade structure presented in [6]
2) The Rusu’s cascade structure presented in [7]
3) Our proposed cascade architecture 2-2 shown in Fig. 2
4) Our proposed cascade architecture 2-1-1 shown in Fig. 4

We have used 1 bit quantizers in all stages of the three architectures. The oversampling ratio has been fixed at 32. The simulations are made using MATLAB. Simulation results presented in Fig. 7, show that our proposed architecture 2-1-1 achieves an improvement of almost 20dB and 10dB in highest attained SNR over Gothenberg’s and Rusu’s architectures respectively.

![Fig. 7. Plot of SNR Vs input signal for four competing cascaded delta-Sigma structures](image)

Table. 1 gives SNRs for four modulators at different values of input signal amplitude to pinpoint the improvement achieved by the proposed structures. Note that Proposed cascade 2-1-1 structure has on the average, an improvement of 4dB and 7dB over Proposed 2-2 and Rusu’s structures, respectively.

<table>
<thead>
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<th>Input</th>
<th>-50</th>
<th>-40</th>
<th>-30</th>
<th>-20</th>
<th>-10</th>
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<tr>
<td>Proposed 2-1-1</td>
<td>52.49</td>
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<td>72.09</td>
<td>82.39</td>
<td>92.36</td>
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<tr>
<td>Proposed 2-2</td>
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<td>58.55</td>
<td>68.6</td>
<td>78.65</td>
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<td>Rusu’s structure</td>
<td>45.56</td>
<td>54.88</td>
<td>65.11</td>
<td>75.34</td>
<td>84.86</td>
</tr>
<tr>
<td>Gothenberg’s structure</td>
<td>45.56</td>
<td>54.88</td>
<td>65.11</td>
<td>74.19</td>
<td>86.76</td>
</tr>
</tbody>
</table>

Table 1. SNRs(dB) for four structures at different values of input(dB)

VI. CONCLUSIONS

Using the simulation results of a single-stage delta-sigma modulator to approximate its quantizer gain, we have established an improved cascaded delta-sigma modulator. Simulation results verify that it attains a very high value of achievable SNR and dynamic range. It has the additional advantages of reduced sensitivity to switch and opamp nonlinearities. We show that by adding a little complexity to the classic cascade architecture, we can achieve high SNR and stable operation for a bigger range of input signals. We only use a bit more complicated digital filter than the one used in the classic architecture to get the improved performance. The results presented in Fig. 4 prove that both the proposed architectures have better dynamic range and achievable SNR than the classic architectures. We get these improved results due to better approximation of quantizer gain; which enables us to design more efficient digital filters which remove the quantization errors more efficiently.

REFERENCES


