An Improved CMOS Class AB First Generation Current Conveyor

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Abstract—It is presented an improved translinear loop based first generation current conveyor (CCI). The proposed CCI is a modified class AB circuit with improved control of the quiescent current and low parasitic input resistance. Performances of the CCI are improved using PSO technique, mainly X-port resistance and current high cut-off frequency. Simulation results are performed to show reached performances.

I. INTRODUCTION

Even though designing CMOS current conveyors suffer from body effect, threshold voltage mismatch between N-channel and P-channel devices and low MOS transistor (MOST) transconductance. CMOS has the important feature of providing complementary devices which allow implementing class AB topologies and particularly class AB current conveyors [1].

Class AB current conveyors offer the advantages of high dynamic range and non-slew rate limited performance. The basic class AB Current lie is shown in figure 1 [2, 3].

A first generation current conveyor can be characterized with the following matrix equation [3]-[6]:

\[
\begin{bmatrix}
  i_y \\
  V_x \\
  i_z
\end{bmatrix} =
\begin{bmatrix}
  0 & \alpha & 0 \\
  \beta & 0 & 0 \\
  0 & \gamma & 0
\end{bmatrix}
\begin{bmatrix}
  V_y \\
  V_x \\
  V_z
\end{bmatrix}
\]

where ideally \(\alpha = \beta = \gamma = 1\), which represent the voltage and current transfer ratios of the CCI.

The current conveyor illustrated by figure 1 suffers from rather poor control of the quiescent current level driving the translinear loop transistor. In addition input port resistances are sources of non-idealities that can drastically affect performances of the current conveyor.

In this paper we propose an improved first generation current conveyor which is a modified version of the one proposed in [2]. It significantly improves control of the quiescent current and presents a low X port parasitic resistance. Besides, bias current and transistor sizes were optimized using the particle swarm optimization technique (PSO) in order to maximize performances of the proposed CCI. Functionality of the optimized CCI is exemplified from a filtering application.

II. IMPROVING THE CCI QUIESCENT CURRENT CONTROL

As Bruun states in [2], first generation current conveyors are usually implemented with a feedback from the X-input branch to the Y-input branch to obtain the input relation \(I_y = I_x\).

In class AB implementation this feedback causes imprecise control of the quiescent current and presents a low X port parasitic resistance. Besides, bias current and transistor sizes were optimized using the particle swarm optimization technique (PSO) in order to maximize performances of the proposed CCI. Functionality of the optimized CCI is exemplified from a filtering application.

Figure 1. Basic class AB Current Conveyor Configuration.

Where transistors \(M_1-M_4\) instantiate the translinear loop. The other transistors form current mirrors.
conditions of the MOSTs. In fact, both current mirror gains as well as MOST conductances are not ideal. This leads to a strong dependency between the quiescent current and \((V_{DD} - V_T)^2\) \[7\] or/and to a stable state with null quiescent current. In addition, it has been proved in \[2\] that the quiescent current is highly sensitive to transistor mismatch in the current mirror.

The idea of stabilizing \(I_0\) consists of feeding back only a fraction of the X-input branch current to the Y-input branch. The remaining part of the current will be provided by added DC current sources \((I_{ctrl})\) to transistors \(M_1\) and \(M_2\). Figure 2 illustrates this approach, where aspect ratios of transistors \(M_5\) and \(M_{13}\) are multiplied by \(\lambda\) and \((1-\lambda)\), respectively. With \(\lambda < 1\).

The quiescent current in each branch can be expressed as follows:

\[
I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{ctrl}}{(1-\lambda)}
\]  

(2)

Where \(I_D\) refers to the drain current of a MOST.

Accordingly, a well controlled quiescent current is obtained unless \((1-\lambda)\) is comparable to device mismatch.

III. IMPROVING X PORT RESISTANCE

In section II we showed that feeding back only a part of the X-branch current to the Y-branch one improves controlling the quiescent current. However, this approach increases the X-input resistance which becomes:

\[
R_X \approx \frac{1-\lambda}{g_{m3} + g_{m4}}
\]  

(3)

instead of \[8\].

\[
R_X \approx \frac{1}{g_{m1}} \left( \frac{g_{o2} + g_{o7}}{g_{o5} + g_{o6}} \right) + \frac{1}{g_{m2}} \left( \frac{g_{o3} + g_{o8}}{g_{o5} + g_{o4}} \right)
\]  

(4)

Where \(g_m\) and \(g_o\) refer to transconductance and conductance of a MOST.

Expressions (3) and (4) show that \(R_X\) of the bias controlled circuit is rather high than the bias controlled one.

In order to lower \(R_X\), a new current path is created which role is to separate the CCI current conveying path from the signal conveying one that presents a low input resistance. This is performed by adding a new current transfer path between the X and Z ports \[9\]-\[11\]. The idea consists of adding a current mirror, i.e. transistor \(M_{17}\) in the (half) circuit illustrated by figure 3.

IV. OPTIMAL SIZING OF THE CCI AND FILTERING

APPLICATION EXAMPLE

A. Optimizing CCI performances

In order to optimize performances of the proposed CCI, mathematical models of X, Y and Z port resistances and current transfer function between X and Z ports were determined. They are given by expressions (5)-(8) respectively.

\[
R_X \approx \frac{g_{o3} g_{o4}}{g_{m17} + g_{m18} + g_{m19} + g_{m20}}
\]  

(5)

\[
R_Y \approx \frac{g_{o5} + g_{o6} + g_{o11} + g_{o12} + g_{o13}}{g_{m1} + g_{m2} + g_{m3} + g_{m4}}
\]  

(6)

\[
R_Z \approx \frac{1}{g_{o19} + g_{o20}}
\]  

(7)
Where Cgs and Cgd refer to the grid to source and grid to drain capacitances of a MOST.

Optimal sizes of the MOSTs and the bias current were determined using the Particle Swarm Optimization technique [12]-[14]. The Pareto front in the hyper space of parasitic resistance and current high cut off frequency was generated. Table I gives ‘optimal’ sizes of each MOS transistor forming the CCI of figure 4. Notice that these sizes correspond to the lower value of Rx of the Pareto boarder.

**TABLE I. OPTIMAL MOSTS ASPECT RATIOS**

<table>
<thead>
<tr>
<th>MOS</th>
<th>Aspect Ratios</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,M3,M8,M12,M16,M18,M20</td>
<td>14.23µm/0.55µm</td>
</tr>
<tr>
<td>M2,M4,M7,M11,M15,M17,M19</td>
<td>24.15µm/0.35µm</td>
</tr>
<tr>
<td>M6,M10</td>
<td>12.80µm/0.55µm</td>
</tr>
<tr>
<td>M9,M5</td>
<td>21.73µm/0.35µm</td>
</tr>
<tr>
<td>M13</td>
<td>02.41µm/0.35µm</td>
</tr>
<tr>
<td>M14</td>
<td>01.42µm/0.55µm</td>
</tr>
</tbody>
</table>

The following SPICE simulations were performed to show performances of the optimized CCI. Simulation conditions are given in Table II. In addition we present in figure 7 the quiescent current in the M3-M4 branch against supply voltage. The quiescent current has obviously been stabilized significantly when compared to the non-stabilized design. In figure 5 we present frequency simulation of the X port resistance for a conventional-non-bias-controlled, the bias controlled and the proposed CCIs. We notice the good improvement of the Rx value when using the proposed design. Indeed for these three CCIs we obtained 71.4Ω, 314Ω and 3.41Ω. In figure 6 we present the frequency current gains, Iz/Ix and Iy/Ix, with a grounded Y port. We notice the good reached current high cutoff frequencies that equal 1.3GHz and 1.8GHz respectively.

**TABLE II. SIMULATION CONDITIONS**

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS AMS 0.35µm</td>
</tr>
<tr>
<td>Voltage supply</td>
<td>-2.5v/+2.5v</td>
</tr>
<tr>
<td>Control bias current (Ictrl)</td>
<td>1µA</td>
</tr>
</tbody>
</table>

Finally we present in figures 8 and 9 DC performances of the proposed CCI, i.e. Spice simulation results of both current errors, (Iy-Ix) and (Iz-Ix), and voltage error (Vx-Vy).

**B. Application Example**

The bias controlled CCI was used in many applications, such as in [15]-[18] for designing CCI-based filters, floating lossless inductances etc. Better performances were reached compared to those obtained using the basic CCI. These performances can be further improved using the proposed CCI. In the following we present an application example of the proposed CCI in order to show its functionality and particularly its high performances. It is a universal voltage...
mode filter taken from [15]. Figure 10 shows this CCI-based filter. In fact it is a dual output universal filter that uses a single CCI. It can provide responses with notch/high pass, high pass/band pass, low pass/band pass or single all pass combinations. In the following we present, as an application example, the output voltage at the CCI Z port. Its transfer function, considering non ideal gains, is given by expression (9).

\[
\frac{V_{outz}}{V_{in}} = \frac{(\alpha - 1)BR_cC_s + (\alpha + \gamma)\beta R_cC_s^2s^2}{\alpha(\alpha - 1)BR_cC_s + (\alpha + \gamma)\beta R_cC_s^2s^2 + (\alpha - 1)R_sC_s + (\alpha + \gamma)\beta R_cC_s^2s^2}
\]

This circuit performs a high pass filter which angular frequency and quality factor are respectively \( \omega_0 = \sqrt{2R_cR_sC_s^2} \) and \( Q = \sqrt{R_c/2R_s} \). For comparison reasons we adopt the same passive element values as those presented in [15], i.e. \( Y_1 : R_1 = 1k\Omega, Y_2 : R_2 = 2.5k\Omega, Y_1 : C_1 = 40pF \) to obtain a filter with a resonant frequency of \( \omega_0 = 1.8MHz \). Figure 11 shows Spice simulation results obtained for the proposed CCI and the one presented in [15]. We also add ideal result obtained using Matlab software.

![Figure 10. CCI-based universal filter.](image)

![Figure 11. Comparisons among the ideal response, the result of [15], and the proposed CCI.](image)

V. CONCLUSION

In this work an improved first generation class AB current conveyor is proposed. It consists of modifying the conventional class AB CCI by adding a quiescent control and a new current conveying path to reduce the X port resistance. Particle swarm optimization technique was used to optimally size the proposed CCI transistors and bias current. Simulation results were performed to show reached performances. The optimized CCI presents a 3.5 \( \Omega \) X-port resistance and 1.3GHz high cut-off frequency. In addition simulation results of a universal filter designed using the optimized proposed CCI were presented and compared to previous published work and also to ideal (Matlab) results.

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