Failure mechanism study and immunity modeling of an embedded analog-to-digital converter based on immunity measurements

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Abstract

In this paper, the failure mechanism of an embedded analog-to-digital converter (ADC) is studied and its immunity modeling with regard to electromagnetic interferences is presented. Failure causes are identified based on off-chip immunity measurements and without specific knowledge of the ADC’s design. Disturbances coupling paths inside the ADC have been recognized as well as the conversion error mechanism. Then, immunity of the ADC is modeled using the ICIM-CI (Integrated Circuit Immunity Model for Conducted Immunity) black-box modeling approach. We show the interest of using the direct power injection (DPI) measurement technique for both analyzing and modeling the immunity of complex integrated circuits.

1. Introduction

Electronic component qualification goes through estimation of their electromagnetic compatibility (EMC) in their functional environments before manufacturing and marketing processes. Due to continuous technological advances of integrated circuits (ICs), these have become more and more miniaturized and complex. Miniaturization of integrated circuit geometrical lengths has led to the reduction of power consumption, and thus noise margins. Mixing digital and analog functions inside the same chip also makes electromagnetic interferences (EMIs) more likely to spread and cause disturbances. As a result, complex ICs with coexisting different functions such as microcontrollers represent a challenge for EMC point of view as interferences can cause critical functional failures.

For integrated circuit designers, it is fully appreciated to have further insight about how to perform an EMC-enhanced design for their circuits in order to obtain good-from-the-first-time products. In this context, several attempts have been recorded to model IC EMC [1]. Predicting the EMC during design phase is valuable for time-to-market reduction by overcoming post-production test and verification processes. As a result, taking into account EMC constraints before manufacturing contributes to improve the efficiency and diminish overall costs. Additionally, understanding the disturbance’s coupling paths inside the chip can give designers some hints about vulnerable areas. Consequently, adequate protection and isolation measures can be taken and implemented during design phase.

In this paper, an embedded analog-to-digital converter (ADC) failure mechanism is studied based on off-chip immunity measurements. Measurement results are used to inspect EMI coupling paths inside the ADC. Then, electromagnetic susceptibility of the ADC is modeled according to a proposed modeling methodology for IC immunity. Section 2 of the paper presents the component under test. Section 3 focuses on the measurement of the ADC immunity characteristics as well as the analysis of its failure mechanisms. Section 4 is dedicated to the construction of the ICIM-CI model of the ADC. Comparisons between measurement results and simulated ones from the developed model are presented. Finally, some conclusions on this work are given.

2. ADC presentation

The studied circuit is a successive-approximation ADC that is embedded in an ATMEL microcontroller (AT90PWM3B). AREF pin corresponds to the conversion reference voltage VREF. The input voltage V_in to be converted, is connected to the ADC through one of its input channels. VREF can be either fed to the ADC from an external source as for VIN or internally generated by a bandgap reference via an internal amplifier [2]. Switching from one reference voltage configuration to the other is done by software programming of a specific microcontroller’s register. In this case study, VREF is internally generated and is equal to 2.56 V. Fig. 1 depicts a block diagram of the ADC. The decimal value of the conversion result is derived as follows:

\[
\text{result} = \frac{V_{\text{in}} \times \left(2^{10} - 1\right)}{V_{\text{REF}}}. \tag{1}
\]
In order to yield the conversion result, three internal blocks act together: the digital-to-analog converter (DAC), the analog comparator and the successive-approximation register (SAR). The latter is initialized with a digital `'1` that is fed into the DAC, which converts this digital code into an equivalent voltage equal to \( V_{REF} \). This voltage is then supplied to the comparator for comparison with the input voltage \( V_{IN} \). When a conversion starts, two successive phases take place at the comparator level. The first one is a locking phase consisting in memorizing \( V_{IN} \) value. This step is executed using a capacitor that is connected to the inverting input of the comparator, which is configured as a voltage buffer by applying a negative feedback. The second phase corresponds to the conversion stage. In this step, the negative feedback is released and \( V_{DAC} \) voltage is routed for comparison with the memorized \( V_{IN} \) voltage. If \( V_{DAC} \) value exceeds \( V_{IN} \), the comparator causes the SAR to reset the initial digital bit; otherwise, the bit is left a `'1`. The next bit is then set to `'1` and the same test is performed until every bit in the SAR is tested. At the end of this 10-step binary search, the resulting code is the digital approximation of the input voltage \( V_{IN} \).

3. ADC failure mechanism

3.1. Immunity measurement

The ADC’s immunity is measured using the DPI (Direct Power Injection) test \([2]\), which consists in injecting an interference signal at the microcontroller’s \( A_{REF} \) pin (\( V_{REF} \) voltage). At the end of the test, susceptibility curves are obtained giving the absorbed power needed to reach a susceptibility criterion and so to consider the ADC as disturbed. The susceptibility criterion has to be representative of a certain disturbance level. Since the ADC’s output is a binary result, it would be suitable to choose the number of lost LSBs (Least Significant Bits) as the immunity criterion for the measurements. An LSB corresponds to the smallest variation in voltage (called quantum) resulting in a change of the decimal conversion result. It is preferable that the immunity criterion is chosen as a power of two so that we can link the disturbance to a precise step among the 10-step conversion process. The decimal result, based on which the number of lost LSBs is estimated, is derived from Eq. (1).

![Fig. 1. Block diagram of the ADC and the reference voltage supply.](image)

![Fig. 2. Immunity measurement results of the ADC.](image)

![Fig. 3. (a) Conversion result distribution and (b) mean conversion value as a function of the disturbance power.](image)

Fig. 2 shows the ADC’s susceptibility curves for different criteria (4, 8, 16, 32 and 64 lost LSBs) in the [1 MHz; 900 MHz] frequency band. For each measurement result, 100 ADC conversions are performed. We consider that the ADC is disturbed according to a specific susceptibility criterion if at least one conversion result is outside the range.

Results of Fig. 2 show first that the immunity of the ADC increases with the interference frequency. Secondly, these results allow distinguishing two different susceptibility zones with regard to the disturbance’s frequency and power level. The first zone corresponds to frequencies up to 30 MHz and power levels below 0 dBm. The second zone corresponds to higher frequencies. These different behaviors of the ADC’s immunity suggest that different failure mechanisms related to each immunity zone may exist.

3.2. Failure mechanism and disturbance coupling paths

In order to better understand the failure mechanism of each of the above-mentioned immunity zones, 100 ADC conversion results for a 16-LSB criterion are depicted in Fig. 3-(a) for 10 MHz (first immunity zone) and 300 MHz (second immunity zone). Fig. 3-(b) presents the mean conversion value as a function of the disturbance power. In this figure, the starting power level \( P_0 \) represents the power at which the

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ADC has been disturbed regarding a 16-LSB susceptibility criterion. Then, power is increased by steps of 1 dBm.

Analyzing results of Fig. 3, we can note that the ADC’s error mechanism in the low frequency zone is rather characterized by a significant dispersion of conversion results while it is rather characterized by the mean value variation at high frequencies. These observations let think that two distinct phenomena take place while disturbing the ADC.

A previous study [3] has shown that the data dispersion is due to the interference, which induces an AC voltage on $V_{\text{DAC}}$ at the input of the comparator (see Fig. 1). Consequently, the conversion gives random results around the theoretical result (equal to 510). The mean variation could be explained by a non-linear effect induced by the interference, which modifies a DC voltage inside the component. Anyway, to better understand this last phenomenon, further investigations have to be carried out. We know that the conversion result computation depends on both $V_{\text{in}}$ and $V_{\text{REF}}$ voltages (see Eq. (1)). Consequently, an alteration of the mean value of these voltages, when the ADC is subjected to an electromagnetic disturbance, results in an error of the conversion mean value. Thereafter, $V_{\text{in}}$ and $V_{\text{REF}}$ voltage variations, as function of the disturbance level, are investigated by measurements. For $V_{\text{REF}}$, the DC variation is estimated as shown in Fig. 4-(a). The RF disturbance is injected to the DUT through a bias tee, whose DC port is connected to a voltmeter to measure the DC variation of $V_{\text{REF}}$. For $V_{\text{in}}$, the AC variation is measured by a voltage probe, which is connected to an oscilloscope (see Fig. 4-(b)). Let’s precise that no significant change in the DC variation of $V_{\text{in}}$ has been measured.

As for the DC variation of $V_{\text{REF}}$ as a function of the absorbed power, it is shown in Fig. 5 for several frequencies. Results show that the conversion reference voltage $V_{\text{REF}}$ is disturbed for all the tested frequencies between 1 MHz and 700 MHz. However, for low frequencies, we need to have a higher power level in order to disturb $V_{\text{REF}}$, in comparison with the power level that is sufficient to disturb the ADC at these frequencies (see Fig. 2).

For instance, let’s look at the 1-MHz curve in Fig. 5. It can be seen that $V_{\text{REF}}$ value starts changing for power levels higher than approximately $-5$ dBm. By making a vertical reading at Fig. 2, it can be observed that at 1 MHz, the disturbance power level does not exceed $-10$ dBm for different susceptibility criteria ranging from 4 to 64 LSBs. We can then conclude that the reference voltage disturbance is not responsible for the ADC’s susceptibility at low frequencies. Therefore, it is possible to suppose that at high frequencies, the disturbance mechanism is mainly due to the modification of the DC component of $V_{\text{REF}}$ voltage. In order to prove this assumption, the number of lost LSBs is compared in Fig. 6 for two chosen frequencies (1 MHz, 700 MHz) belonging each to a susceptibility zone. Red curves represent measurement results obtained by making vertical readings of Fig. 2. Blue curves represent the number of lost LSBs that would have been obtained if we had considered the supposed hypothesis; i.e. the conversion error is caused by the reference voltage variation. For each power level, the corresponding $V_{\text{REF}}$ is taken from Fig. 5 results and the decimal conversion result is computed using Eq. (1) and initial $V_{\text{in}}$ value. Then, subtracting the conversion result before disturbance from the one obtained with disturbed $V_{\text{REF}}$ gives us an estimation of the number of lost LSBs.

Results confirm the previous finding as to the presence of two ADC immunity zones. In fact, at 1 MHz (first immunity zone), there is no correlation between the reference voltage disturbance and the ADC failure. However, at 700 MHz, we obtained a good agreement between different curves.

This observation has been made for most of the tested frequencies. Moreover, it has also been noticed that a coupling path exists between $V_{\text{REF}}$ and $V_{\text{in}}$ pins, inducing an AC component on $V_{\text{in}}$, voltage when a disturbance is injected. Fig. 7 presents the AC variation of $V_{\text{in}}$ for different frequencies covering the whole measurement frequency band. Considering the high amplitude of this AC component for some few frequencies (500 MHz for example), it has been concluded that for these frequencies, the AC variation of $V_{\text{in}}$ may play a role in the ADC disturbance even in the high-frequency zone.

The presented study on the ADC’s failure mechanism allowed us to draw up a clearer picture, shown in Fig. 8, of the disturbance coupling paths inside the chip, hence complementing the previous study on the same ADC [3].

4. ADC immunity modeling

4.1. ICIM-CI model construction

Once the ADC’s failure mechanism and disturbance coupling paths have been studied, we present in this section the ADC’s immunity modeling according to the Integrated Circuit Immunity Model for Conducted Immunity (ICIM-CI). ICIM model is currently a work item proposal for standardization under the IEC 62433 project dealing with modeling aspects of ICs emission and immunity. ICIM-CI model [4] consists in offering a generic methodology allowing the creation of an immunity model for an electronic component. The model is composed of two blocks, which are the PDN and the IB. It is illustrated in Fig. 9.
The passive distribution network (PDN) block makes the link between the external RF disturbances and the internal residual ones while the immunity behavior (IB) block models the circuit’s response to an electromagnetic disturbance.

In our study, the PDN block is extracted using a vector network analyzer (VNA). The tested pin’s input impedance is determined by a one-port S-parameter measurement. The IB block consists in developing analytical functions to describe the correlation between DPI results for different test frequencies. Fig. 10 illustrates the DPI-derived ICIM-CI model with a behavioral IB block.

In order to build the IB block following the above-mentioned methodology, DPI measurement results need to be plotted in a certain way, showing the number of lost LSBs as function of the disturbance power. Vertical readings of Fig. 2 results are sufficient to get the appropriate representation. Fig. 11 depicts the obtained plots for frequencies between 1 MHz and 500 MHz. Having observed Fig. 11 plots, it seems possible to model the results as lines using Eq. (2):

\[ \text{LostLSBs} = a(f_i) \times P_{\text{DPPI}} + b(f_i) \]  

(2)

where \( a(f_i) \) and \( b(f_i) \) are the line’s coefficients for the frequency \( f_i \) (1 ≤ \( i \) ≤ 13).

In order to compute the number of lost LSBs, we need first to determine the absorbed power \( P_{\text{abs}} \) which corresponds to the disturbance power \( P_{\text{DPPI}} \) in Eq. (2). More precisely, the absorbed power can be computed as follows:

\[ P_{\text{abs}} = P_{\text{inj}} \left( 1 - |S_{11}|^2 \right) \]  

(3)

where \( P_{\text{inj}} \) is the injected power and \( S_{11} \) is the reflection coefficient of the tested IC’s pin.

The next step of building the IB block consists in recovering different ‘a’ and ‘b’ coefficients corresponding to different frequencies. These coefficients are extracted after having done a fitting of Fig. 11 results. Then, a second fitting is performed to determine analytical functions describing different coefficients variation with frequency. This has been obtained using polynomial functions as can be seen in Eqs. (4) and (5):

\[ a(f) = \sum_{i=0}^{m} x_i f^i \]  

(4)

\[ b(f) = \sum_{i=0}^{m} y_i f^i \]  

(5)

Fig. 6. Number of lost LSBs for two disturbance frequencies: (a) 1 MHz and (b) 700 MHz.

Fig. 7. \( V_{\text{in}} \) AC variation with power level.

Fig. 8. Disturbance coupling paths inside the microcontroller.

Fig. 9. ICIM-CI model structure.
4.2. Comparison between measurement and modeling results

Once the model built, the immunity curves simulated from the model are compared to the DPI curves obtained by measurements. Fig. 12-(a) and (b) shows a comparison between the injected power ($P_{\text{inj}}$) and the absorbed power ($P_{\text{DPI}}$) measurements from one side and modeling susceptibility curves from another side, respectively for a 16-LSB criterion.

A good agreement between measurement and modeling results is obtained. For some frequencies, modeling results exhibit some discrepancy. In fact, these differences are due to the uncertainty of polynomial functions that are used to compute $a'$ and $b'$ coefficients for these frequencies. Actually, these results prove that different fittings that have been performed, especially for DPI results, are quite satisfactory. Results of Fig. 12-(a) show that the model-extracted injected powers are realistic which validates the developed ICIM-CI model for the ADC’s immunity.

5. Conclusions

In this paper, the failure mechanism analysis of an embedded ADC has been presented. The advantage of this study’s approach is that it is relying on off-chip immunity measurements. Then, we showed a useful methodology for black-box immunity modeling using the proposed ICIM-CI structure. In the case of the studied analog-to-digital converter, immunity measurements proved to be practical for giving further insight on the internal failure causes as well as producing consistent immunity models.

Acknowledgments

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References

[2] IEC 62132-4, Direct RF Power Injection to measure the immunity against conducted RF-disturbances of integrated circuits up to 1 GHz, IEC Standard 2003.