Numerical analysis and experimental tests for solder joints power cycling optimization

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1. Introduction

Power device packaging evolved rapidly in the last decade, both in terms of technological solutions (see for instance at the 3D integration [1]) and materials (plastics, ceramics, lead-free solders). Such evolution makes mandatory a corresponding progress in the thermo-mechanical reliability test conditions, which cannot be considered as a well-established topic, but have to be adapted as a function of the various packaging solutions.

Power cycling is the most realistic stress test for thermo-mechanical failure mechanisms. Recent publications on power cycling lifetime models for IGBT power modules have demonstrated the impact of pulse duration on the cycling lifetime of chip-near interconnections (chip-to-substrate solder, Al wire bonds). In [2] a statistical analysis of a significant number of power cycling tests was conducted but, since it only yields a total number of cycles until failure, without taking into account the existence of different end-of-life failure modes, not a clear dependence on the power-on time \( t_{on} \) was obtained. In [3,4] power cycling on modules fabricated with different bond-wire and die attach technologies were done, in order to isolate different failure modes (pure lift-off, bond heel cracking, die attach degradation), and for every one of them the dependence on \( \Delta T \) and \( t_{on} \) was analyzed. In [5], the impact of the maximum junction temperature on bond wire lift-off and die-attach degradation was addressed.

All these works were focused on power modules and studied the failure mechanisms related to the internal device structure, such as wire bonding and die attach. However, the reliability of external solder joints [6,7] is still a key issue in the reliability of a power converter using discrete packaged devices, since they represent the mechanical, electrical, and thermal connections between the power device and the board.

Although it was widely studied for decades, new research effort is required considering new materials employed for solders (lead-free) and boards (such as IMS — Insulated Metal Substrate [8]), and new mounting structures.

In a previous work [9] we developed a thermo-mechanical FE model for a SO8 packaged power MOSFET mounted on a board by lead-free solder joints. In contrast with other larger power packages such as D²Pak, in which the thermo-mechanically weakest point during power cycling was demonstrated to be at the die attach [10], for SO8 bondless packages the edge of the external solder joints was found as the thermo-mechanically critical point [9]. On the basis of these simulations, in the present paper, in order to focus our attention to the reliability of external solder joints of packaged devices, a SO8 bondless power MOSFET was chosen as carrier device, and a methodology was set for the choice of power cycling parameters.

To fix the test conditions (power source, cycle period, duty-cycle, cooling) a detailed numerical thermal model of the whole device/package/board assembly is necessary, in order to:

- find the thermally critical points in the assembly;
- limit the maximum temperature reached by the semiconductor device;
- know the temperature at every device section;
- obtain the required temperature swing at the solder joints, with a cycle period as lower as possible;
- be sure that the test condition does not introduce other failure mechanisms in the device under test;
- know the agreement between the temperatures at every device section with the one chosen for monitoring.

Here, the described numerical model is applied to a specific device/package/board configuration, in order to set the proper parameters for power cycling. Experimental tests were carried out to validate the numerical model.
2. Power cycling parameters

It is well known that temperature excursion ($\Delta T$) activates thermo-mechanical failure mechanisms. There are two classes of accelerated tests for power electronics: thermal cycling [11] and power cycling [12]. In thermal cycling the device under test is placed in a system able to force continuous and relatively fast (from tenths of seconds to minutes) ambient temperature changes. In power cycling self-heating of the device is obtained by operating it at severe power conditions (ON-phase), and cooling it (by natural or forced convection) during the OFF-phase. In power cycling the heat is generated inside the device and flows towards the ambient, as in the real operation, then the stress conditions better reproduce those experienced in the actual application.

In order to get statistical data enough for realistic extrapolation, accelerated life-tests at different values of $\Delta T$ have to be performed. Since the results are not given in terms of time-to-failure, but in terms of number-of-cycles-to-failure, it is possible to shorten as much as possible the duration of the test by a proper choice of the stress parameters:

• ON-phase power rating: it is the typical parameter used to set $\Delta T$;
• cycle period: the longer the period, the higher the $\Delta T$ and the larger the interested region in the whole assembly but, obviously, the longer the test;
• selective forced air cooling: can be activated during the OFF-phase to shorten it, but it increases the complexity of the experimental set-up;
• duty-cycle: in the case of not symmetrical thermal time constants (see for instance the case of selective forced air cooling), it can be increased from 50% to a higher level, together with a ON-phase power increase (when possible), to shorten the whole period.

Although various attempts were done along the years, a standard procedure to set the proper parameters for power cycling, for any failure mechanisms, and any types of package, was never established. The procedure here proposed tries to fill this lack by using steady-state and time dependent FE thermal modeling of the specific device/package/board.

3. FEM thermal modeling of the device/board assembly

Since among the purposes of this work there is the a priori determination of optimum cycle from the point of view of the acceleration of fatigue damage in solder joints, considering the indications obtained in [9] about thermo-mechanical stress, here a FE model was developed to simulate only the thermal behavior of the SO8 packaged device mounted on the PCB. The transient analysis of this model can be used to choose the ON-phase power rating, the period and the duty cycle.

To focus the attention on the external solder joints stress, avoiding bonding wire reliability problems, a bondless device was selected as test vehicle. The device under test was a SO8 discrete 17A/30V power MOSFET. Fig. 1 shows the 3D structure of the device soldered on a testing board. The product specification sheet given by the manufacturer of the power MOSFET has been used for geometric details. The same sheet was helpful to identify the materials of this device and to set their thermal properties. Since the interest was not on the intrinsic semiconductor device, this was considered as a homogeneous layer of silicon generating a uniform power per volume unit inside the die. The PCB was made using a standard 1.6 mm thick FR4 with single sided 1 oz (thickness 35 $\mu$m) copper. For the sake of simplicity, a stress bench without a selective forced cooling was made, then in the FE model the boundary conditions were set as natural air convection on the whole external surfaces. The FE thermal model is essentially the same developed in [9], where more details about it can be found. What is new here is its use, to obtain information about the temperature swing at the solder joints by varying the stress cycle parameters.

3.1. Simulation results

The steady-state analysis was the starting point, used to set the maximum $\Delta T$ achievable at the solder joints at the maximum power rating. Instead, transient simulations were performed to evaluate the best trade-off between dissipated power, period, and duty-cycle. For instance, the maximum $\Delta T$ of 102 °C is achievable with a 5 min long ON-phase, at $P_0 = 1.22$ W, when the thermal steady-state conditions are almost reached. Fig. 2 shows the simulated external temperature map after 5 min with a dissipated power of 1.22 W.

The period could be shortened of about 20% by properly increasing the convective heat transfer coefficient (forced air) during the OFF-phase, but this option was not yet experimentally implemented, since it would require to split the test bench and to twice the IR acquisition system.

Here a digression can be done about the possibility of using the simulation to find proper parameters for other failure mechanisms. For instance, if one is interested in die attach degradation, short pulses (in the range of tenth of ms) are the best choice to set fast accelerated tests without affecting the reliability of external solder joints. For example, in this case, with a dissipated power of 100 W during a 30 ms long pulse (at the limit of the SOA reported on data-sheet), the die temperature (and similarly the one of the die-attach) increases of 75 °C, while the temperature of the solder joints increases only of 20 °C (see Fig. 3). Fig. 4 shows the thermal transient, in the above conditions, at the top of the package (where temperature is monitored by IR-camera in the experimental setup), the die, and one of the external pins. It is evident that such pulse could be repeated with a period of 20 s, without appreciable pin temperature increase.

We simulated also other periods and dissipated power values, starting from a period of 10 min to reach and stay some minutes at the steady-state with $P_0 = 1$ W. In this case the increase of the solder joints’ temperature is around 90 °C, as can be seen in [9].
Fig. 5 shows the results in some points of interest with a period of 2 min and PD = 1 W. As can be seen, in this case the temperature at the top of the package is almost the same of one in the silicon die. The temperature increase at pins (around 60 °C) is not so high to get a satisfactory acceleration, then we made other simulations and measurements to obtain higher temperature increases.

4. Experimental

4.1. The power cycling automatic test bench

In order to verify the simulation results and to perform stress test experiments, an automatic test bench was set up, starting from the one presented in [9], and making on it the following changes:

- IR temperature measurement was added also at the end of the cooling phase;
- the range of the IR camera was modified in order to allow measurement of temperatures higher than 120 °C;
- variable duty-cycle has been enabled;
- a mechanical structure was designed and built for fixing the board and for millimetric adjustment of the IR camera position;
- the IR image was calibrated in the measuring temperature range in order to correct emission coefficient variations;
- a thermocouple was added and calibrated for ambient temperature measurement;
- the Labview control software was enhanced with some features, such as automatic plot of temperature diagrams, ambient temperature monitoring, automatic formatting and saving of collected data.

Fig. 6 reports the test bench block diagram, while a picture of the experimental set-up is shown in Fig. 7. We used an Agilent E3631A power supply, a National Instruments DAQ NI USB 6361, two solid-state relays (60 VDC, 20 A), a FLIR A325 IR-camera, and a Linear Technology LTK001 as thermocouple cold junction compensator with matched amplifier to measure the ambient temperature.

Fig. 6. Block diagram of the power cycling test set-up.

Fig. 7. The power cycling test set-up.
It may be noted that the most expensive component of this bench is the IR-camera, but it is not strictly necessary. A video camera that grabs up to 60 frame/s is underutilized, because the procedure requires only pictures taken on time intervals of a minute or more. Then, a cheaper bench can be built, without lowering its performances.

4.2. Power cycling parameter set-up

Power cycling was performed on the test board already presented in [9], on which 16 S08 MOSFETs were soldered by 95.5Sn–4.0Ag–0.5Cu alloy. Four of them (which means 32 solder joints), connected in parallel two by two (as illustrated in Fig. 6), were stressed at different conditions:

- dissipated power (0.98 and 1.22 W);
- cycle period (2, 4, 10, 20 min);
- duty-cycle (40% and 50%).

Table 1 reports the measurement results (temperature at the end of ON and OFF phases and ΔT), once the thermal regime is reached. The 20 minute period case is not listed, since it does not show relevant differences with the 10 min one.

As an example, Fig. 8 shows the temperature on the top of the package measured and simulated (only the first cycle) during power cycling with a period of 2 min and a dissipated power of 1 W.

The good agreement obtained between measurements and simulations demonstrates the effectiveness of the presented procedure for the power cycling parameter optimization in the case of thermo-mechanical mechanisms affecting the external solder joints.

<table>
<thead>
<tr>
<th>PD [W]</th>
<th>tON, tOFF [s]</th>
<th>TON [°C]</th>
<th>TOFF [°C]</th>
<th>ΔT [°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.98</td>
<td>60, 60</td>
<td>101</td>
<td>35</td>
<td>66</td>
</tr>
<tr>
<td></td>
<td>120, 120</td>
<td>102</td>
<td>29</td>
<td>73</td>
</tr>
<tr>
<td></td>
<td>300, 300</td>
<td>107</td>
<td>27</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td>48, 72</td>
<td>97</td>
<td>32</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td>96, 144</td>
<td>100</td>
<td>26</td>
<td>73</td>
</tr>
<tr>
<td></td>
<td>240, 360</td>
<td>104</td>
<td>25</td>
<td>79</td>
</tr>
<tr>
<td>1.22</td>
<td>60, 60</td>
<td>121</td>
<td>36</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td>120, 120</td>
<td>127</td>
<td>32</td>
<td>95</td>
</tr>
<tr>
<td></td>
<td>300, 300</td>
<td>130</td>
<td>28</td>
<td>102</td>
</tr>
<tr>
<td></td>
<td>48, 72</td>
<td>118</td>
<td>34</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td>96, 144</td>
<td>124</td>
<td>30</td>
<td>94</td>
</tr>
<tr>
<td></td>
<td>240, 360</td>
<td>130</td>
<td>27</td>
<td>103</td>
</tr>
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4.3. Early power cycling test results

Fig. 9 shows the measured VDS across the four MOSFETs at the end of the ON-state phase, during the first 14,292 cycles performed until now, with PD = 1.22 W and period = 2 min. It can be observed that this voltage is almost the same for all the transistors and that it is not constant. The VDS variations are due to the ambient temperature excursions in the laboratory where we used the bench (day and night, and change of season). Spikes are due to thermal regime recovery after some stops and restarts of the test. Similar variations can be observed in the measured temperatures, but they disappear in ΔT (Fig. 10).

The power cycling is at very early stage and no damage to the joints was obviously still observed. Optical analysis with a microscope over the 32 solder joints under test was performed at the beginning and it is scheduled after every 50,000 cycles, or when a device fails.

5. Conclusions

In this work a procedure to set the proper parameters for power cycling was developed. It is firstly based on FE modeling of the device/package/board assembly. It was applied to the case of solder joints of SMD power devices and experimental results were presented, showing a good agreement with simulations. Such a procedure allows to choose the power level and tON in order to obtain the wanted ΔT on the solder joints, and to perform the greatest number of cycles as possible within the shortest possible time, and this was the main goal of this work.

Moreover, power cycling is now in progress and preliminary results are shown in the paper.
References


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