Impact of hot carrier injection on switching time evolution for power RF LDMOS after accelerated tests

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ABSTRACT

This paper investigates the effects of hot carrier injection on the switching performance of power RF LDMOS (Radio Frequency Lateral Diffused Metal–Oxide–Semiconductor) devices. In addition, their influences on the dynamic parameters are studied after various accelerated aging tests (thermal and electrical). The response of these parameters and the switching waveform are described. The findings of experimental results are presented and discussed. Measurements show that important variations are obtained on the devices’ rise time. After aging tests, the charge trapping in the gate oxide causes the modifications in the Miller capacity level and width resulting in an increase of the rise time and a decrease in the fall time, consequently increasing of the switching losses.

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1. Introduction

Power MOSFETs have widely used in applications space systems, particularly in DC/DC power conversion. The major interest for industry, mainly space industry is the use of the devices that can withstand high temperature and/or high voltage operations, where we need to avoid the use of large cooling systems. MOSFET devices are very fast switchers and they are widely used in the industry because they provide at the same time a combination of fast switching and low on-resistance [1].

The switching time variations of power MOSFETs are still on the agenda from the reliability point of view because the gate oxide degradation effects the switching characteristics. The electrical and/or thermal stress changes the interface and oxide charges into the gate oxide and these charges cause degradation in power MOSFETs parameters such as threshold voltage, mobility and terminal capacitances which alter the switching parameters [2]. Due to the increased demand on reliability and safe operation, it is necessary to investigate the MOSFET devices behavior under various running conditions. The work methodology consists in characterizing the device parameters before and after aging, for comparing their performances under various test conditions.

The switching speed evolution of MOSFETs is seldom studied from the reliability viewpoint, knowing that the oxide charge effect does not exclude the altering of switching parameters [3]. The electrical parameters evolution and their relation with the oxide layer charge after various accelerated aging tests were largely studied in [4,5]. Particularly, the dynamic parameter drifts of power RF LDMOS devices. We investigated in this work, the switching times and dynamic parameters of MOSFET devices after accelerated tests.

The content of this paper is presented as follows: Section 2 describes the experimental characterization set-up and the general LDMOS transistor performances. The discussion and results are shown in Section 3. The conclusion and prospects is given in Section 4.

2. Characterization and experiment setup – general power RF LDMOS transistor performances

The buck converter structure is represented in Fig. 1. To characterize the switching waveform and the voltage switching period (VSP) we use a particular circuit which is representative of the static converter circuits: a series chopper (buck). This circuit is a DC/DC converter but it is also found in the arms of an inverter, so it is also representative of the DC/AC energy conversion. It has the following specifications: power supply = 25 V; output voltage = 12.5 V; power = 10 W; commutation frequency \( f = 50 \) kHz; and duty cycle = 50%.

The switching cell is constituted by an RF-LDMOS transistor and a Schottky diode across the DC motor. For the device characteristics, no disappearances are observed.

The RF-LDMOS device under test is a commercial telecom dedicated transistor (encapsulated in a 2-lead flange package with a ceramic cap) S-band operating and 65 V DC biasing. Indeed, these performances are given in conditions of width pulse 500 \( \mu \)s with a duty cycle of 50%. The
The gate length is equal to 0.8 μm. The junction temperature does not exceed 150 °C for a flange temperature equal to 65 °C. The thermal resistance is 0.2 C/W.

For this study, the devices are stressed with an applied drain-source voltage (Vds) of 40 V and a gate-source voltage (Vgs) necessary to obtain a permanent drain-source current (Ids) less than 20 mA (without self-heating effect), which corresponds to the quiescent current at ambient temperature. The transistors have been characterized before and after aging tests following [5,8]:

* Transistors after thermal aging (Thermal Cycling Tests: TCT), on which 10 thermal cycles without interruption of 10 min for each cycle (from −75 °C to 75 °C with ΔT = 150 °C) without DC bias (Fig. 2) [5,14].
* Transistors after DC electrical aging (High Voltage Drain: HVD), where a Vds voltage equal to 40 V and a Vgs voltage equal to 3.5 V during 15 h are applied. The conditions are investigated in order to establish an unequivocal conclusion on the comparison of the different tests (Table 1).

A modified structure of RF power N channel LDMOS, previously developed by Raman et al. [6], was implemented and simulated using the physical simulator Atlas of Silvaco [7]. Fig. 3 shows the device's structure with approximate doping wells. The main geometrical and technological parameters are given in Table 2.

### Table 1

<table>
<thead>
<tr>
<th>Test</th>
<th>Temperatures</th>
<th>ΔT</th>
<th>Ids at Tamb</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCT</td>
<td>−75 °C/+75 °C</td>
<td>150 °C</td>
<td>Without DC</td>
</tr>
<tr>
<td>HVD</td>
<td>Tamb</td>
<td></td>
<td>3 mA</td>
</tr>
</tbody>
</table>

The implemented structure is typically similar to our tested device. Consequently the qualitative understanding of physical phenomenon will be studied. The suggested structure has a Gaussian doping profile along LDD and channel surface. The doping profile was optimized using a technological process simulation carried out by SSUPREM3 [7,13], see Fig. 3.

### 3. Results and discussion

Fig. 4 presents the comparison between the Vds(t) switching waveform at the cell bound before and after aging test. The switching losses are changed (see Table 3) but the devices are still in their specified range after test. Under these conditions, the electrical test induces faster degradation than the thermal test.

Fig. 5 shows the aging influence and the rise time (time taken by a signal to change from a low value to a specified high value) parameter degradation at the cell bound of Vds waveform switching. Table 3 presents the rise time evolution and fall time after each aging test. We note that rise time increases depending of aging. The electrical aging test induces major degradation of rise time than in the thermal aging. Fig. 6 presents the fall time (the time taken for the amplitude decrease from a value to another specified value) degradation of Vds waveform with various accelerated aging tests.

The power RF LDMOS switching begins by charging the gate-channel capacity in order to invert the semiconductor surface when the gate voltage is above the threshold voltage. Table 4 presents, the peak amplitude evolution at resonant frequency (9 MHz) before and after aging and also the values of the largest increases in the spectra. This is given at the transistor's Turn-ON and Turn-OFF. Study [5] shows that these aging tests of power RF LDMOS devices causes a degradation in electrical parameters such as: threshold voltage, Cgd, Cgs and Crss (see Table 5) [5,8].

These parameter shift due to change of physical properties caused by hot-carrier effect [5,10,11], thereafter affecting in both on the switching time. The study presented in [1] shows the aging component which can have another effect: the stressed device reduces the rise time; thereafter, it will decrease the Cgd capacitance of 31% after electrical aging [5] (see Table 5). In the chopper application, the most important capacitance for dynamic behavior is Cgd [12,13]. Precisely, they showed...
that an increase in the value of the Cgd caused a decrease in both the amplitudes and the resonance frequencies of the spectra. It dominates the output switching waveforms through the ‘Miller’ effects. The switching performance shifts in the power LDMOSFET can bring changes in the primary voltage and current[9]. The transient performance of the power device changed after stress. The power efficiency is related to this regime of the switching devices[9].

Therefore, according to the previous works[12,13], this important decrease of the Cgd value explains the switching time shift observed. The decrease in the capacitances (Cgd and Crss) after thermal aging is lower than after electric aging[10]. This explains why the increase of the switching time shifts is more important after electric aging than after thermal aging.

The electric parameters of MOS transistor are more and more sensitive to defects bound to the presence of charges in the gate oxide and at the Si/SiO2 interface[5,10]. According to the literature[1,5,11], the cause and the origin of the observed shift related to the presence of very high electric field that increases carrier injection into the grown silicon dioxide layer (SiO2) and into interface state Si/SiO2[5,15]. The detail of the lateral electric field distribution of the active silicon layer in channel and drift regions is shown in Fig. 7, using a physical simulation software (Silvaco-Atlas, 2D). This strong electric field causes the generation of charge states at the silicon–oxide interface[9,16].

The hot carrier degradation effect is closely related with current density and with the total number of free electrons at the silicon–oxide interface, where most of the electrons are concentrated deep inside the drift region[15–17].

Hence, the electron concentration contours across the active silicon layer can be observed from Fig. 8. It could be noticed that the concentration is very high at the gate level, on the right (drain side) in such a way that it provides a significant increase of the surface current density at the gate edge. Consequently, many electrons are accelerated to high velocities by this high electric field peak. They become highly energized and should be accelerated away from their normal directional flow.

In other words, the drain–source voltage increases the electric field in the drift region and near the oxide layer, therefore enhancing the trapping process. So, the degradation[14,18] is attributed to hot electron-induced interface state generation and/or impact ionization.

Table 2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source length</td>
<td>1.1</td>
</tr>
<tr>
<td>Source-gate spacing</td>
<td>1</td>
</tr>
<tr>
<td>Gate length</td>
<td>0.8</td>
</tr>
<tr>
<td>Gate-drain spacing</td>
<td>3</td>
</tr>
<tr>
<td>Drain length</td>
<td>1.1</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>0.065</td>
</tr>
</tbody>
</table>

Table 3

<table>
<thead>
<tr>
<th></th>
<th>Before aging</th>
<th>Thermal</th>
<th>Electrical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td></td>
<td>%</td>
<td>%</td>
</tr>
<tr>
<td>Rise time (10^{-6}s)</td>
<td>1.012</td>
<td>1.006</td>
<td>6.016</td>
</tr>
<tr>
<td>Fall time (10^{-7}s)</td>
<td>5.217</td>
<td>5.191</td>
<td>1.019</td>
</tr>
</tbody>
</table>
4. Conclusion and prospects

The results obtained for power RF LDMOS devices highlighted that switching time shifts are important in electrical aging tests. Stressing that, during one switching period, the rise time degradation is faster and more important than fall time. The gate oxide of the devices is subjected to high field in order to induce defects in the oxide layer, and/or at the Si/SiO\textsubscript{2} interface. This phenomenon degrades the physical behavior of device, thereby the critical dynamic parameters (C\textsubscript{gd} and C\textsubscript{oss}); that are sensitive to the electrons injected in gate/SiO\textsubscript{2} interface traps. These charges affect the switching parameters by increasing the rise time and by decreasing the fall time. The switching performance study of power RF LDMOS devices shows that it is sensitive to oxide degradation.

These problems are of major concern for power MOSFETs performance and can be solved via the driving stage. Extensive tests for switching are needed to improve the overall converter reliability. The experimental results will be followed and confirmed by a detailed simulation analysis. Moreover, it would be interesting to make the connection with the normal life of a component, through an aging model or MTTF (mean time to failure) if we have all data. The comparison of this study with other technologies such as IGBT and VDMOS is underway.

Table 4
Peak amplitude evolution (dB mV) before and after aging at resonance frequency (9 MHz).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Before aging</th>
<th>After aging</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Thermal</td>
<td>Electrical</td>
</tr>
<tr>
<td></td>
<td>Value ΔV</td>
<td>ΔV</td>
</tr>
<tr>
<td>Turn-OFF</td>
<td>11.31</td>
<td>20.47</td>
</tr>
<tr>
<td></td>
<td>+ 9.16</td>
<td>+ 22.47</td>
</tr>
<tr>
<td>Turn-ON</td>
<td>15.36</td>
<td>17.2</td>
</tr>
<tr>
<td></td>
<td>+ 1.87</td>
<td>+ 17.47</td>
</tr>
<tr>
<td>All period</td>
<td>18.37</td>
<td>24.81</td>
</tr>
<tr>
<td></td>
<td>+ 6.44</td>
<td>+ 36.59</td>
</tr>
<tr>
<td></td>
<td>+ 18.62</td>
<td></td>
</tr>
</tbody>
</table>

Table 5
Dynamic parameter values variations obtained after aging tests (%: percentage change).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Before aging</th>
<th>After aging</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Thermal</td>
<td>Electrical</td>
</tr>
<tr>
<td></td>
<td>Value %</td>
<td>Value %</td>
</tr>
<tr>
<td>C\textsubscript{ox} (pF)</td>
<td>2.73</td>
<td>2.72</td>
</tr>
<tr>
<td>V\textsubscript{ds} = 0 V</td>
<td>0.36</td>
<td>2.60</td>
</tr>
<tr>
<td>28 V</td>
<td>4.76</td>
<td></td>
</tr>
<tr>
<td>C\textsubscript{pp} (pF)</td>
<td>0.57</td>
<td>0.57</td>
</tr>
<tr>
<td>V\textsubscript{gs} = −1.5 V</td>
<td>0</td>
<td>0.50</td>
</tr>
<tr>
<td>0.57</td>
<td>12.3</td>
<td></td>
</tr>
<tr>
<td>C\textsubscript{pp} (pF)</td>
<td>12.5</td>
<td>12.5</td>
</tr>
<tr>
<td>V\text{gs} = 0 V</td>
<td>12.5</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Fig. 7. Lateral electric field distribution in N-LDMOS structure, with V\textsubscript{ds} = 40 V and V\textsubscript{gs} = 3.5 V bias.

Fig. 8. Electron concentration distribution of N-LDMOS, with V\textsubscript{ds} = 40 V and V\textsubscript{gs} = 3.5 V bias.

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References