A robust electro-thermal IGBT SPICE model: Application to short-circuit protection circuit design

D. Cavaiuolo, M. Riccio, L. Maresca, A. Iracé, G. Breglio, D. Daprà, C. Sanfilippo, L. Merlin

**Abstract**

An optimized electro-thermal IGBT SPICE model based on the Kraus model was developed to allow reliable simulation at application level. A particular emphasis to the temperature dependence of physical parameters was given for both the on-state and breakdown conditions. The model was experimentally validated in steady state and transient operation on a Field-Stop trench-gate 30 A–600 V commercial IGBT device. The effectiveness of the convergence–accuracy aspects was proved for the proposed model. The application to the short-circuit protection circuit design for a hard switched fault in an inverter motor-drive application was also analysed. The ability of the proposed IGBT model was experimentally verified with a simplified-equivalent circuit where a short condition was forced on the load, enabling the desaturation protection by the IGBT driver. The results show an accurate prediction of the device electro-thermal behaviour under short-circuit conditions, with a possible optimal design of the desaturation circuit parameters when the device experiences hard-switched-fault or fault-under-load events.

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**1. Introduction**

Nowadays a careful choice and design of IGBT short-circuit (SC) protection circuits have become crucial [1,2] also because in some application device may experience many non-destructive SC events [3]. In this scenario, the abrupt increase of junction temperature may significantly reduce the device lifetime expectancy according to the theorized models [4]. Unfortunately, design of protection circuit parameters is actually performed according to datasheet and application notes, which provide a general approach and rough design rules, neglecting device technological specificity and self-heating effect: therefore, the optimal design cannot be pursued. Consequently, accurate electro-thermal (ET) simulations of IGBT under SC condition [5] would be very effective for protection circuit design. Besides numerical TCAD simulations, where detailed information on the device structure are needed, a valid solution can be the use of SPICE simulations with coupled electrical and thermal networks [6]. Unfortunately, despite a very high number of compact IGBT models proposed in literature, only two models are implemented within SPICE simulators as built-in library: the NIGBT model, based on the Hefner model [7], included in PSpice OrCad® and the HiSIM model [8] implemented in ELDO SPICE®. Furthermore, IGBT manufacturers provide itself SPICE sub-circuits to simulate his products, where a drastic trade-off between convergence and accuracy is present [9]. Hence, in this paper, we propose an accuracy-convergence optimized IGBT SPICE model, that accounts for self-heating effect, with the aim of evaluating the impact of a well-aimed protection circuit design on device reliability.

**2. IGBT SPICE model**

The model we propose is an enhanced version of the Kraus model [10], optimized for PSpice implementation. A remarkable improvement concern the addition of a linear-region transconductance factor \( K_f \) adopted in Hefner model for reproducing the PiN–BJT combined effect of trench-gate IGTBs [7]. The equation for the MOSFET current becomes the following:

\[
\begin{align*}
\Phi_{BCH} &= \frac{K_f K_p}{2} \left( \frac{V_{gs} - V_{th}}{V_{ds} - \frac{V_{gs}^2}{2}} \right), \\
K_f V_{ds} &= V_{ds} \left( V_{gs} - \frac{V_{th}}{2} \right).
\end{align*}
\]

The current expression includes the effects of the high transverse electric field for high gate voltage is also been included through the parameter \( \Phi \). Hence, it’s possible to implement the Hefner approach for modelling the PiN effect in Kraus PSpice model by only means of a simple modification: the internal IGBT \( V_{ds} \) voltage is multiplied by \( K_f \) and then imposed as drain-source voltage across the Level 1 MOSFET model through the a controlled voltage source.
Furthermore, other important enhancements regard the introduction of Miller temperature-dependent avalanche modelling [7]:

$$M_{nv} = \frac{1}{1 - \left( \frac{V_{cb}}{BV_{ce}(T)} \right)^\beta}$$

the use of explicitly evaluated solution for steady-state carriers charge $Q_{b0}$ aimed to model optimization [11] and the definition of temperature dependencies for physical parameters in case of trench-gate devices [12].

The new model was validated on a Field Stop (FS) trench-gate 30 A–600 V commercial IGBT and the algorithm proposed in [13] is used to effectively evaluate the model parameters. In order to identify the main properties and the improvements brought by new model, it is compared with sub-circuit based model provided by manufacturer and NIGBT model present in the OrcAD Pspice library. In Fig. 1 an overview of the main performance characteristics for the three considered SPICE models is given. Apart the comparative evaluation of the accuracy, the speed and the convergence of the model, other features were evaluated. The physics accounts for the number of formulas involved in the models; the parameters accounts for the number of physical parameters of the models; the extensibility accounts for the number of parameters that can be customized; the simplicity accounts for the inverse of the computational complexity of the model. In particular results from DC characteristics, along with inductive load turn-off transient are normalized and reported in Fig. 1. The other parameters are evaluated by the thorough evaluation of the model equations and implementation in SPICE like simulator. Simulation results are compared to the experimental ones.

The device measured-simulated DC characteristics and turn-off transient voltages and current waveforms at $T_j = 27^\circ$C depicted in Fig. 2a–b reveal the goodness of the improved model respect to NIGBT and manufacturer models.

Moreover, the effectiveness of new model is also confirmed by comparison of simulated IGBT blocking characteristics (Fig. 3a) and inductive turn-off transient collector current waveforms (Fig. 3b) at increasing operative temperature with experimental ones.

3. Short-circuit test ET simulation

The first circuit application considered as a case-study for new PSpice ET model validation, is the standard short-circuit (SC) test, that is usually performed by device users in order to verify its capability to sustain both high-voltage and high-current values, before destructive thermal runaway event occurs. The simplified schematic of experimental short-circuit test setup used for ET simulations is depicted in Fig. 4. A Foster equivalent thermal network provided by the device manufacturer on the device datasheet, was used in PSpice simulation in order to investigate the transient behaviour of junction temperature.

The test conditions are as follows: $V_{GE} = -5/15 \, V$, $R_G = 10 \, \Omega$ and $T_{j0} = 27^\circ$C. Fig. 5 reports the comparison between experimental waveforms of DUT short-circuit collector current and collector-to-emitter voltage during an SC pulse of $\tau_{SC} = 5 \, \mu s$, since it’s guaranteed on the datasheet as the maximum short-circuit time interval before device failure. The results prove that the new PSpice model is capable to accurately predict the ET behaviour for the DUT.

4. Short-circuit protection circuit design

As a case study for the model validation, we consider an inverter for motor-drive application, where two main kinds of short-circuit conditions may occur: a shoot-through of the leg or a short of the load (Fig. 7a). Nevertheless, since experimental characterization of IGBT SC in application is very tricky to deal with, the effectiveness of the model in this condition is proved by means of a simplified-equivalent experimental circuit. In a step-down converter, a short is forced on the load and a SC event occurs on the conducting IGBT, enabling the desaturation protection by the driver HCPL-316J, provided by Avago Technologies®.

In this case the well-known desaturation method is considered, which consists on the sense of device saturation collector-to-emitter
During normal condition, IGBT operates in linear region, so its collector-to-emitter voltage is small: if a short-circuit event occurs, its collector current $I_C$ abruptly arises till saturation region, where the $V_{CE}$ voltage becomes larger. When the value of $V_{CE}$ exceeds a defined threshold value, the digital control detects a “fault condition” and forces the “soft” turn-off of the IGBT. The sense circuit is depicted in Fig. 6 and the logic circuits needed to achieve device protection are all integrated within the IGBT gate-driver. However, it is required the design of some external desaturation circuit parameters such as $V_{ce,th}$. 

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**Fig. 3.** Model comparison on a) IGBT blocking characteristic and b) simulated-measured IGBT turn-off collector current inductive turn-off IGBT current waveform at $V_{cc} = 400$ V, $L = 30$ A, $R = 10$ Ω and $L = 250$ μH VS $T_j$.

**Fig. 4.** PSpice OrCad equivalent schematics of short-circuit test experimental setup.

**Fig. 5.** DUT measured and simulated a) current and b) voltage waveforms during SC test at $TSC = 5$ μs, $VCC = 360$ V, $V_{CE} = −5$ V, $R_o = 10$ Ω, $T_j = 27$ °C.

**Fig. 6.** Simplified schematic of desaturation circuit $V_{ce}$ detection by means $V_{desat}$ voltage.

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PARAMETERS:

- $V_{dc} = 350$
- $T_J = 27$
- $R_g = 3.3$
- $V_{ge} = 10$
- $t_{sc} = 10u$

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C\text{\text{blank}} or R\text{\text{pull-down}} according to IGBT characteristics in order to prevent device from critical SC electro-thermal conditions which may affect its reliability and lifetime. The typology of SC event is classifiable as a HSF ("hard switched fault" [14]) and the total path inductance is quite high (L\text{wires} = 1.9 \mu H) due to the wires of the link to the motor. The circuit (Fig. 7b) is simulated in PSpice OrCad® environment and the equivalent Foster model of device-package thermal network is taken from device manufacturer datasheet, assuming T\text{case} = T\text{amb}. The simulated IGBT current–voltage waveforms using the new model (Fig. 8) show a better accordance with experimental data respect to the NIGBT model, while the manufacturer provided model is not even able to achieve convergence in this kind of electrical network.

The electro-thermal validation of the model was performed in stationary conditions. More in detail, the step-down converter topology (see Fig. 7b) was analysed in non-fault conditions and the simulated mean value for \Delta T\text{j} was compared with the experimental measurements (a hole was made, through the plastic coverage, to achieve the die surface in order to directly measure the T\text{j} mean value).

In particular, the steady-state device junction temperature reaches about T\text{j} \approx 55 °C (both measured and simulated), proving that the temperature dependence on IGBT saturation current value is properly taking into account with new model. On the other hand, the differences in gate voltage behaviour, especially after desaturation sensing, are due to "soft" dynamic turn-off control of the gate by the driver, not suitably reproduced by the NIGBT model. Hence, the proposed IGBT model allows to accurately predicting device behaviour under SC conditions, therefore it is possible to optimally designed desaturation circuit parameters when the device experiences HSF or FUL SC events.

On the other hand, when the path inductance is small and the current rise-time become very short, a delay on circuit protection response is present. A formula for C\text{\text{blank}} rough evaluation is given in gate-driver datasheet: once a t\text{\text{blank}} time before fault detection is defined, the C\text{\text{blank}} is estimated from the internal desaturation current I\text{ch} and the desaturation voltage threshold V\text{\text{desat}} according to the following expression:

\[
C_{\text{blank}} = \frac{t_{\text{\text{blank}}} I_{\text{ch}}}{V_{\text{\text{desat}}}}. \tag{3}
\]

Usually a practical value of t\text{\text{blank}} equal to 1.5 \mu s is recommended to avoid protection circuit false activation, and the corresponding C\text{\text{blank}} is 47 pF, if I\text{ch} = 250 \mu A and V\text{\text{desat}} = 7 V are considered. This design method do not consider the self-heating effect and the device physics specifications. With this simplified design of the SC protection circuit, the device may experiences large \Delta T\text{j} during short-circuit time interval. This appears clear from simulation results of an HSF IGBT short-circuit event, where the higher is the C\text{\text{blank}} value for avoiding false activation of desaturation circuit, the higher is also the time interval before protection intervenes when SC occurs, with the consequence of abrupt increase of device junction temperature (Fig. 9).

Another example of design optimization using electro-thermal SPICE IGBT model regards the wise choice of R\text{\text{goff}} when the driver circuit does not provide an embedded "soft" control of the gate voltage turn-off (Fig. 10).

The R\text{\text{goff}} value can be accurately selected in order to limit the over-voltage due to stray inductances when turning-off high short-circuit current according to device speed characteristics (tail current and lifetime). Using a fast and accurate IGBT ET model we can predict the...
behaviour of collect-emitter peak voltage versus $R_{goff}$ for different values of stray inductance, when a shoot-through occurs to a single leg of an inverter (Fig. 6). For instance, in the analysed case the device can experience a breakdown avalanche event for a $R_{goff} < 25 \Omega$ under 200 nH stray inductance.

5. Conclusions

An optimized ET IGBT SPICE model based on the Kraus model was developed and experimentally verified on a Field-Stop trench-gate 30 A–600 V commercial IGBT device. The application to the short-circuit protection circuit design for a hard switched fault in an inverter motor-drive application was also analysed. The results showed an accurate prediction of the device electro-thermal behaviour under short-circuit conditions, with a possible optimal design of the desaturation circuit parameters when the device experiences hard-switched-fault or fault-under-load events.

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