Effects of thermal and electrical stress on DH4T-based organic thin-film-transistors with PMMA gate dielectrics

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1. Introduction

In the past decade, a lot of research effort has been dedicated to organic thin-film-transistors (OTFTs), and, thanks to their continuous improvement, they are gaining more and more attention. OTFTs have many advantages in terms of costs with respect to their silicon counterparts, especially in large-area devices, such as displays. In fact, there are many inexpensive deposition techniques, which are well suited for large area and require processing temperature, which is lower than that needed to grow amorphous and polysilicon TFTs [1–5]. Besides, organic materials are compatible with a large variety of plastic substrates, which are lighter, less brittle, and less expensive than glass. Plastic substrates can also be bent, making OTFT an enabling technology for many applications such as smart textiles or flexible displays [2,5,6].

Unfortunately, despite the huge improvement in terms of performances [1–6], many stability and reliability issues are still present, preventing their widespread commercial use. For instance organic TFTs are sensitive to environment factors such as moisture, oxygen and other contaminants [7–10] and to light or UV exposure [11–25].

Organic TFTs may also suffer from charge trapping, if a prolonged high bias is applied, as it has been widely discussed in the literature [24–37]. Furthermore, besides reversible charge trapping, bias stress might also induce permanent degradation either in the gate dielectric or in the organic semiconductor [24,26,27]. In the literature, large attention has been paid to the bias stress instability and permanent degradation, however, the combined effect of bias and temperature on the degradation kinetics is still a relatively unexplored field.

In this work, we investigate the effects of the temperature and bias stress on fully-organic p-type OTFTs. We compare the effects of pure thermal stress and pure bias stress (at room temperature) with the effects of simultaneous bias and temperature.

2. Experimental and devices

Throughout this work, we analyzed p-type all-organic thin-film transistors, whose structure is shown in Fig. 1. Devices were fabricated in bottom gate–top contact configuration, on glass substrates with gate contact consisting of a 150 nm thick ITO layer. A PMMA layer (450 nm) was spin-coated on top of ITO as dielectric layer. A 15 nm thick dihexyl-quaterthiophene (DH4T) semiconductor layer was deposited by physical vapor deposition (PVD) at 0.015 nm/s. Finally, 70 nm thick gold drain and source electrodes were deposited on top of the stack at 0.1 nm/s. OTFTs’ channel width was 12 mm, while channel length was 70 μm. The devices are encapsulated in nitrogen atmosphere with glass covers, to avoid degradation due to air exposure. To reduce the effects of residual contaminations, DryFlex® getters from SAES Getters S.p.A. were employed.

We considered three different stress procedures, which were applied to different, nominally equal, sets of samples. The first procedure (thermal stress, hereafter) is a staircase thermal stress: after the initial characterization (performed at 20 °C), the device is brought at a desired stress temperature (iTstress) and it is kept for 1000 s, with no bias applied. After that, the device’s temperature is brought again to 20 °C and a new characterization is performed. This stress-characterization sequence is repeated, increasing each time the stress temperature by 5 °C. The whole procedure begins with iTstress = 35 °C and it ends after the characterization performed after the 80 °C stress (see Fig. 2). In the second procedure, the device is subjected to a similar staircase thermal stress,
but it is also biased with $V_{CS} = -80\, \text{V}$ and $V_{DS} = 0\, \text{V}$ (electro-thermal stress, hereafter) in the ON state. In the third procedure (constant voltage stress, CVS hereafter), the device is stressed with the same bias ($V_{CS} = -80\, \text{V}$ and $V_{DS} = 0\, \text{V}$) of the electro-thermal stress, but $T_{\text{stress}}$ is always kept at 20 °C, until a 10,000-s cumulative stress time is reached. Electrical bias, when present, was performed in the ON-state, as we found that it induces the largest degradation [36,37].

Device characterization includes the transfer (ID–VGS) and output characteristics, and the ID–VGS taken with $V_{DS} = V_{GS}$ (diode connection, ISAT hereafter).

3. Results and discussions

In Fig. 3, we show the transfer characteristics (ID–VGS) taken at different stress steps for different stress procedures. Noticeably, the different stress types induced different degradation kinetics. For instance, the device subjected only to thermal stress featured an initial degradation, followed by a recovery and, lastly, a new degradation cycle (see Fig. 3a). The device subjected to a pure electrical stress (Fig. 3b) showed a progressive leftward shift of the electrical characteristics, accompanied to a moderate stretch-out. Both the stretch-out and the leftward shift are much more pronounced if thermal stress is simultaneously applied (Fig. 3c). These different behaviors can be also noticed in the output characteristics taken at $V_{GS} = -80\, \text{V}$, and plotted in Fig. 4 for different stress conditions.

To better analyze the stress effects, we calculated from the diode-connection ISAT curve the threshold voltage variation ($\Delta V_{\text{TH}}$) and the mobility ($\mu$), using the model of Ref. [38]. The evolutions of these parameters are shown in Figs. 5–7, where we also show the evolution of the saturation drain current.

The threshold voltage evolution (see Fig. 5) depends on the stress procedure: it constantly decreases if bias is applied (see triangles and circles in Fig. 5). The rate at which the threshold voltage decreases is larger if the device is heated during the stress. The larger threshold voltage variation on the device subjected to simultaneous heating and bias could be ascribed to the higher temperature (pure CVS stress is performed at 20 °C). In fact, temperature could enhance ionic motion in the PMMA layer or it could favor charge injection in PMMA traps. Nonetheless, the temperature can also enhance the stress-induced trap generation rate. Those traps, closer to the interface, contribute to the final value of the threshold voltage.

When only thermal stress is performed, the threshold voltage initially decreases (see squares in Fig. 5), but later, at high temperatures, it starts reaching its fresh value (i.e. $\Delta V_{\text{TH}} = 0$). This recovery on the threshold voltage does not occur if bias is applied during thermal stress, because drift of ions or charged particles may also occur with bias. The
small threshold voltage variation during the pure thermal stress is not unexpected: in fact, during the characterization, the device is subjected to $V_{GS}$ values up to $-80$ V (even if for a time much shorter than 1000 s). Therefore, during the characterization, some charges could be trapped. Later, when the stress temperature increases, part of the trapped charges is detrapped, favored by thermal emission. Incidentally, DH4T phase transition occurs at about 60 °C [39], and we think that the reorganization of the semiconductor layer could have effects not only on the trapped charges/traps but also on the mobility, which will be discussed in the following.

The mobility variation also shows different kinetics (see Fig. 6). For instance, it is constantly decreasing in the devices subjected only to electrical stress at a 20 °C constant temperature (see triangles of Fig. 6). The devices subjected also to simultaneous thermal stress showed an increased initial degradation of the mobility (see circles of Fig. 6). Later, at high temperatures, there is a saturation on the degradation kinetics and even a small partial recovery. The partial recovery might be induced by some sort of annealing, induced by the moderately high temperatures. In fact, on one hand, high temperature might accelerate the effects of the bias stress, on the other hand, they might induce a partial recovery, i.e. by recrystallization, when the device is brought back to 20 °C for characterization.

Instead, when just thermal stress is applied, the degradation is not monotonic and two turnarounds appear (see squares in Fig. 6). Initially, the measurements induce small but still measureable mobility degradation. Later, the larger temperature (around 60 °C) induces a partial annealing, which mitigates some of the damage caused by the high electric field during characterization. However, when the temperature reaches 75 °C, it induces some permanent degradation, instead of annealing. At this point, one might wonder why the high temperature induced a further degradation on devices not subjected to bias, whereas it even induced a partial recovery on the mobility on devices subjected also to electrical stress. The answer might be the different damage the device suffered, before reaching 75 °C. In fact, at 75 °C the device not subjected to electrical stress almost retained 90% of its carrier mobility, i.e. it has not been strongly degraded. On the other hand, the device subjected to simultaneous thermal and electrical stress almost lost 80% of its mobility, indicating that it has been seriously degraded, therefore
the effects of the recrystallization could overwhelm the additional degradation induced by stress and temperature. Still, we expect that at even higher temperature, the degradation might overwhelm any sort of annealing.

The saturation drain current, shown in Fig. 7, depends on both the threshold voltage and the mobility, and it decreases if electrical stress is performed (see triangles in Fig. 7). The variation is much more pronounced, if heating is simultaneously applied to the device (see circles in Fig. 7). However, in case of pure thermal stress, we observe a settling (or even a partial recovery) of the saturation drain current at the higher temperatures reached in this work (see squares in Fig. 7). This is due to the partial mitigation between competing phenomena. In fact, between 55 and 70 °C, the threshold voltage decreases (i.e. it increases in absolute value) causing a reduction of the drain current. In the same range, however, the mobility starts increasing, resulting in an almost constant \( I_{\text{SAT}} \).

The opposite trend occurs on both the threshold voltage and mobility, between 70 °C and 80 °C: we observe an increasing threshold voltage variation (due to a net negative trapped charge variation) and a decreasing mobility. Still, these variations partially compensate each other, and \( I_{\text{SAT}} \) features only marginal variations (in particular, we observed a small increase). Due to limited variations on the threshold voltage and mobility on devices subjected to pure electrical stress, the saturation drain current variation is large, but still below 40% of its initial value. However, when simultaneous heat and bias are applied, the saturation drain current quickly decreases below 1% of its initial value, due to the simultaneous degradation of mobility and threshold voltage.

At this point some considerations are worthy to be drawn. We observe a limited variation of the characteristics if the device is kept unbiased and heated up to 80 °C. Similarly, we observed larger but still limited variations if the devices are kept at 20 °C and subjected to bias. The most striking phenomenon is the strong temperature acceleration of bias stress, which quickly degrades the device performances even at considerably small temperature values. The degradation might not only be intrinsic to DH4T, but also to the PMMA layer, or it might derive from the interaction between the DH4T and contaminants. Such contaminants might be either process-induced or they could come from the external environment, penetrating the glass sealant. Thankfully, the getter might substantially reduce the effects of contaminants. This poses some serious concerns on the integration of DH4T in devices meant to be operated at even moderately high temperatures (60 °C). Proper cooling techniques or precaution must be adopted to avoid the simultaneous action of bias and temperature. Noticeably, this problem does not only occur in high temperature environments (or when the device is exposed to

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normalized \( I_{\text{SAT}}(h)/I_{\text{SAT}}(0) \)

\[ \begin{array}{|c|c|c|c|c|c|c|c|c|}
\hline
\text{Stress time [x10^3 s]} & \text{CVS@20°C} & \text{Thermal stress} & \text{Thermal + CVS} \\
\hline
1 & 1.0 & 1.0 & 1.0 \\
2 & 0.8 & 0.8 & 0.8 \\
3 & 0.6 & 0.6 & 0.6 \\
4 & 0.4 & 0.4 & 0.4 \\
5 & 0.2 & 0.2 & 0.2 \\
6 & 0.0 & 0.0 & 0.0 \\
7 & 0.0 & 0.0 & 0.0 \\
8 & 0.0 & 0.0 & 0.0 \\
9 & 0.0 & 0.0 & 0.0 \\
10 & 0.0 & 0.0 & 0.0 \\
\hline
\end{array} \]

\[ \text{Stress Temperature } T_{\text{stress}} \text{ [°C]} \]

4. Conclusions

We performed thermal and bias stress in encapsulated p-type oligothiophene OTFTs with a PMMA layer as gate dielectric. The devices exhibited very different behaviors, depending on the stress conditions. Very limited variations were observed if the devices were subjected only to thermal or electrical stress. However strong degradation occurred on both mobility, threshold voltage and saturation drain current, when the devices were subjected to simultaneous thermal and electrical stress.

Other aspects are worth to be investigated, among them we may cite:

- the long-term stability of the damage, i.e., if this degradation is permanent;
- the effects of other bias configurations (e.g. OFF state, saturation, pulsed gate/drain stress), which might show additional unexpected issues;
- the effects of temperature transients, which might induce phase transition on the materials;
- the effects of bias stress at lower temperatures (even below 0 °C);
- the determination of a safe operating area as a function of the device temperature.
- the analysis of different semiconductors and gate dielectric materials, in particular, the analysis on n-type OTFTs.

These and other issues should be assed to have a comprehensive scenario.

References


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