Impact of gate insulator on the dc and dynamic performance of AlGaN/GaN MIS-HEMTs

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A B S T R A C T

This paper studies the impact of the properties of the SiN gate insulator on the dc and dynamic performance of AlGaN/GaN Metal Insulator Semiconductor High Electron Mobility Transistors (MIS-HEMTs). We compare the dynamic and transient behaviour of devices with identical epitaxial structure and different gate insulators: RTCVD-SiN (rapid-thermal-chemical-vapour-deposition) and PEALD-SiN (plasma-enhanced-atomic-layer-deposition).

We demonstrate the following important results: (i) the gate leakage of devices with PEALD-SiN insulator is three orders of magnitude lower than that of samples with RTCVD-SiN; (ii) the use of PEALD-SiN reduces significantly the transistor threshold voltage hysteresis; (iii) both sets of samples show measurable threshold voltage shift when submitted to forward gate bias. In addition we demonstrate (iv) that the VTH shift is well correlated with the gate forward leakage and bias, for both sets of samples. This result indicates that trapping is induced by the injection of electrons in the gate insulator when a positive bias is applied to the gate; in PEALD SiN devices, the reduction of the gate (forward) leakage results in a significant decrease in VTH shift.

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1. Introduction

Over the last decade GaN based High Electron Mobility Transistors (HEMTs) demonstrated remarkable performance in applications which require high frequency and power [1,2]. Excellent properties in terms of breakdown voltage, operation at high temperature and superior electron mobility make them a very interesting solution in these areas.

Significant efforts were done in order to further reduce reliability issues, e.g. high leakage current and trapping phenomena, revealing interesting solutions such as metal–insulator–semiconductor HEMTs (MIS-HEMTs). Furthermore MIS-HEMT structures should avoid several degradation mechanisms peculiar of Schottky junctions [3,4]. Recent papers demonstrated a significant performance in MIS-HEMTs in terms of both the reduction of forward and reverse gate currents [5,6] even at high temperature [7] and in terms of reliability toward off-state [8] and on-state stress [9].

However, although the superior characteristics reached, devices are still affected by significant trapping phenomena. Previous results demonstrated the impact of the high drain bias and hot electrons, induced during off-state bias and semi-on-state bias respectively, on the dynamic on-resistance increase [8,10] and its correlation, during off-state condition, with the buffer vertical leakage current and the gate-drain length [7,11]. An analysis of MIS-HEMT slow trapping phenomena moreover demonstrated that significant trapping effects (e.g. VTH shift) are induced by positive gate voltage, suggesting the presence of traps between AlGaN barrier and dielectric under the gate [12–15]. This result is partially confirmed by Lin et al. [16].

Lagger et al. [17] discuss the impact of a different dielectric material (LPCVD SiN, SiO2, Al2O3, HfO2, HfSiO2) and thickness on the VTH shift and on the density of trapped electrons Ntr when a forward gate bias stress is performed.

Nevertheless, to date little investigation has been performed concerning the impact of the different gate properties of the SiN gate insulator on the dc and dynamic performance of AlGaN/GaN MIS-HEMTs and on the correlation between them when a forward gate bias is applied.

The aim of this paper is to investigate the impact of a different gate dielectric deposition (e.g. rapid-thermal-chemical-vapour-deposition (RTCV) SiN and plasma-enhanced-atomic-layer-deposition (PEALD) SiN) on the device performance and to provide a description of trapping mechanisms when the devices are submitted to a forward gate bias.

2. Experimental details

The study was performed on d-mode gate recessed MIS-HEMTs grown on a 200 mm-diameter Si substrate (Fig. 1). Devices are characterized by the same epitaxial structure, which consists of a AlN nucleation layer (200 nm), an AlGaN buffer layer (2.3 μm), a GaN
channel (150 nm), and an Al$_{0.22}$Ga$_{0.78}$N barrier layer (3.7 nm remaining under gate dielectric) with a GaN cap layer. The two sets of samples differ for the gate insulator: 15 nm RTCVD-SiN (rapid-thermal-chemical-vapour-deposition) — sample A and 15 nm PEALD-SiN (plasma-enhanced-atomic-layer-deposition) — sample B.

After a preliminary dc characterization, pulsed analysis was performed by means of a custom setup: I–V characteristics are defined by pulsing both terminals from several trapping conditions or quiescent bias points ($V_{GSO}$, $V_{DSO}$) [18]. In order to avoid self-heating effects a pulse width of 1 μs with a duty cycle of 1% is used. Slow trapping phenomena are analysed by means of drain current transients (DCTs). The device is kept in a trapping (or detrapping) bias condition for 1000 s; the drain current corresponding variation is monitored in the access regions, but, according to $V_{TH}$ dynamic shift, they take place under the gate region.

### 3. Experimental results

#### 3.1. Impact of SiN passivation on dc performance

Fig. 2 compares the gate-source diode current measured on devices with RTCVD-SiN and PEALD-SiN gate insulator. It demonstrates that, in both cases, a MIS-HEMT structure reduces significantly both reverse and forward gate currents. Furthermore it proves that PEALD-SiN induces a measurable improvement in the forward gate current, more than three orders of magnitude lower than in RTCVD-SiN samples.

**Fig. 2.** Comparison of gate-source diode current measured on devices with different gate insulators: RTCVD-SiN (black curve) and PEALD-SiN (red curve). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

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3.2. Effects of SiN passivation on trapping behaviour

Fig. 4 demonstrates that the gate insulator determines different trapping effects both when reverse bias and forward bias are applied during quiescent bias points. In the first case (reverse bias) RTCVD-SiN samples demonstrate a negative $V_{TH}$ dynamic shift ($\approx 500$ mV) and a max $\beta_{in}$ dynamic slight decrease ($\approx 25$ ms/mm). The PEALD-SiN devices reveal significant improvements, demonstrating no significant dynamic variation in similar conditions.

A positive voltage bias ($V_{GSO} > 0$ V) determines a significant variation of current collapse in both sets of samples; current dispersion is mainly ascribed to $V_{TH}$ dynamic shift. Differently from RTCVD-SiN samples, PEALD-SiN samples demonstrate to be less sensitive, revealing significant $V_{TH}$ shift only for $V_{GSO} > 4$ V.

**Fig. 3.** Comparison of transfer characteristics ($I_D$ vs $V_G$) measured on devices with different gate insulators: RTCVD-SiN (a) and PEALD-SiN (b). Evaluation of $V_{TH}$ hysteresis in knee voltage ($V_{GSO} = 2$ V) and saturation zone ($V_{DS} = 10$ V).

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**Fig. 5.** Demonstrates that, in both cases, a positive voltage bias induces a negligible dynamic transconductance peak decrease. We can therefore suggest that, during a forward bias, trapping phenomena do not occur in the access regions, but, according to $V_{TH}$ dynamic shift, they take place under the gate region.
4. Discussion about results

4.1. Correlation between trapping and gate current

Fig. 6 confirms that RTCVD-SiN devices reveal a measurable $V_{TH}$ dynamic positive shift with $V_{GSQ} > 0$ V. If we consider the $V_{TH}$ variation for $V_{GSQ} > 2$ V (due to parameter analyser sensitivity), we prove that the $V_{TH}$ dynamic shift is well correlated to the forward gate current.

Fig. 7 shows that RTCVD-SiN and PEALD-SiN sets of devices similarly behave for positive voltage bias, although with different sensitiveness. The comparison of $V_{TH}$ dynamic shift measured in the two sets of devices demonstrates significant improvements in PEALD-SiN devices.

If we compare $V_{TH}$ dynamic shift at the same $V_{GSQ}$ (e.g. $V_{GSQ} = 5$ V), PEALD-SiN devices prove a $V_{TH}$ shift reduction of more than 2.5 V. Indeed, no measurable variation is noticed up to $V_{GSQ} = 4$ V. A variation of less than 500 mV is measured at the maximum operating voltage ($V_{GSQ} = 5$ V). If a further $V_{GSQ}$ is applied, a good correlation between the $V_{TH}$ dynamic shift and the gate-source diode current is noticed, too.

Fig. 8 proves that, both in RTCVD-SiN and PEALD-SiN devices, the $V_{TH}$ dynamic shift linearly increases with the gate forward current. Gate current values lower than 50 pA/mm were not considered due to instrumentation sensitiveness.

Furthermore, Fig. 8 proves that, if we compare $V_{TH}$ dynamic shift at the same gate forward current value, PEALD-SiN devices demonstrate a lower $V_{TH}$ shift ($\approx 0.5–1$ V).

If we consider the band bending at different $V_{GSQ}$ applied, we can therefore speculate that, with $V_{GSQ} > 0$ V, trapping can be induced by the injection of electrons in the gate insulator. This condition is promoted both by $V_{GSQ} > 0$ V and by a significant flowing of the forward gate current. Therefore, in PEALD-SiN devices, the reduction of the gate (forward) leakage results also in a significant decrease in $V_{TH}$ shift.

Fig. 6. Evaluation of the gate-source diode current as a function of the gate voltage applied ($V_{GS}$) and of the threshold voltage ($V_{TH}$) dynamic shift as a function of a different gate voltage applied during the quiescent bias point ($V_{GSQ}$). Device with RTCVD-SiN gate insulator is considered.
Results are confirmed by drain current transients (DCTs) measured in consistent bias points. Fig. 9(a) shows DCT capture kinetics induced by different quiescent bias points and monitored at high power dissipation conditions in knee voltage zone in RTCVD-SiN samples. Fig. 9(b) describes the corresponding recovery (emission) transients monitored in consistent bias point.

DCT analysis confirms pulsed analysis results: the increase of $V_{GSQ}$ during trapping kinetics, and thus of gate forward current, enhances electron capture mechanisms. According to pulsed analysis, the drain current decrease is mainly ascribed to $V_{TH}$ shift when a forward gate bias is applied.

DCT evaluation explains that transients are influenced, during capture and emission kinetics, by both fast and slow traps.

DCT analysis on PEALD-SiN samples (not shown here) reports consistent results to pulsed measurements and confirms capture kinetics induced by consistent gate forward current levels. When $V_{GSQ}$ lower than 4 V is applied, a little drain current decrease is measured even after 1000 s ($\leq 15\%$ at $V_{CSQ} = 3$ V, $V_{DSQ} = 0$ V), mainly ascribed to a slight $V_{TH}$ shift.

5. Conclusions

This paper investigates the impact of the SiN gate dielectric on the dc and dynamic performance of AlGaN/GaN MIS-HEMTs, through the comparison of RTCVD-SiN and PEALD-SiN structures.

Results demonstrate that a PEALD-SiN gate insulator induces significant improvements on dc properties in terms of reduction of the gate forward current (three orders of magnitude) and $V_{TH}$ hysteresis.

PEALD-SiN gate insulator results in significant improvements also in terms of trapping effects: differently from RTCVD-SiN structures a reverse bias induces no dynamic variation (e.g. $V_{TH}$ shift, $\Delta gm$ decrease); a forward gate bias induces no $V_{TH}$ shift up to $V_{GSQ} = 4$ V, resulting in a much lower sensitiveness to $V_{CSQ}$ than RTCVD-SiN structures.

Dynamic and dc properties are well correlated, proving that in both structures $V_{TH}$ dynamic shift increases with the gate forward current. PEALD-SiN devices demonstrate when the same $V_{CSQ}$ and gate forward current are respectively considered, a $V_{TH}$ dynamic shift of 2.5 V and 0.5–1 V lower than RTCVD-SiN samples.
DCT evaluation confirms results, confirming that both fast and slow trapping mechanisms contribute to capture and recovery kinetics. Trapping analysis suggests that a $V_{CGS} > 0$ V and the flowing of forward gate current promote trapping phenomena, induced by the injection of electrons in the gate insulator.

References


