Characteristics and aging of PCB embedded power electronics

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Abstract

The decrease of battery prices makes the electrification of the power train an irresistible development. Also the introduction of a 48 V on-board grid is decided to supply large auxiliaries. For such applications cost is always an important factor.

PCB embedded power electronics offers improvements compared to power electronics bonded and soldered on Al₂O₃ as dielectric material. These improvements are a reduction of height, lightweight construction, cost efficiency of the applied materials and a reduction of the parasitic inductance. Sinter layers offer an increase of the melting temperature from 220 to 935 °C, compared to solder, and the thermal resistance between semiconductor and cooling water is low due to a thin dielectric layer of 150 μm and the heat spreading inside the copper leadframe, together with PCB materials having a thermal conductivity of 1.5 W/mK. A thermal resistance of 0.5 K/W per IGBT can be achieved. This paper describes the challenges of the production process, the 5 μm copper metallization of the semiconductor and the sinter process. Production failures were detected by curve tracer measurements, lock-in thermography and cross sections. The application potential of the embedding technology is demonstrated by measurements of the thermal impedance and temperature dependent partial discharge measurements. The effect of aging of PCB material by thermal cycling on the partial discharge behavior could be demonstrated. First results of an ongoing power cycling measurement are described as well. Finally the aspect of new PCB material without glass-fiber enforcement offering higher thermal conductivity and higher glass-transition-temperature is shown.

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1. Introduction

PCB embedded power electronics offers improvements compared to power electronics bonded and soldered on Al₂O₃ as dielectric material [1,2]. These improvements are smaller size, lightweight construction, cost efficiency of the applied materials and low parasitic inductances [3,7]. First products for application below 60 V are already in production [11]. The thermal resistance between semiconductor and cooling water can be lower due to a thin dielectric layer of 150 μm and the heat spreading inside the copper leadframe, together with new PCB materials having a thermal conductivity of up to 7 W/mK [4]. This paper describes the challenges of the production process, the copper metallization of the semiconductor, the sinter process and the impact of the embedding on the semiconductor. Device failures were detected by curve tracer measurements, lock-in thermography and cross sections.

Final test samples are characterized by measurements of the thermal impedance and temperature dependent partial discharge measurements. The effect of aging of PCB material by thermal cycling on the thermal impedance and temperature dependent partial discharge measurements.

Fig. 1. Construction in cross section: areas of interest are marked in red. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

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http://dx.doi.org/10.1016/j.microrel.2015.06.072
0026-2714/© 2015 Published by Elsevier Ltd.
partial discharge behavior could be demonstrated. First results of an ongoing power cycling measurement are described as well. Finally the aspect of new PCB material of higher thermal conductivity and higher glass-transition-temperature and without glass-fiber-enforcement is shown.

2. Composition

A 650 V IGBT with an area of 1 cm² is sintered onto a 6 to 10 times thicker copper leadframe, seen in Fig. 1. The semiconductor has a 5 to 10 μm thick copper layer on top. The top side connections like gate and emitter are contacted by copper vias through the PCB material.

As dielectric material, a 150 μm PCB layer is used between collector and cooler. The whole PCB board can be sintered onto the cooler. The load current is contacted by press-fit connectors.

3. Top side copper layer

To achieve a good connection between copper via and IGBT, an 8 μm thick copper layer was created on the top side of the IGBT. First, the copper was sputtered onto the IGBT. In cross sections of the copper layer it can be seen, that the layer is reproducing the topology on top of the IGBT, see Fig. 2. Also grain boundaries are created during sputtering.

One PCB fabrication process step called “brown-oxide” etching is used to roughen the copper surfaces for a better connection between copper and epoxy resin.

During this process, acid liquids are flowing between grain boundaries and remove about 2 μm copper off the surface. As a result of this process, the copper and the aluminum metallization on top of the IGBT are partially removed, see Fig. 3.

In an improved process, a 5 μm copper layer was galvanic deposited. Fig. 4 shows a plane copper layer after processing, and a 3 μm thick, but also plane remaining copper layer after the “brown-oxide” process.

4. Sinter process

In a first run, semiconductors were sintered onto a copper leadframe. As top metallization of the leadframe, a 600 nm thick chemical silver layer was chosen. First the sinter-paste was placed onto the leadframe, then the semiconductor was placed onto the sinter-paste. This process showed difficulties in the positioning of sinter-paste and semiconductor. It became apparent that where sinter-pastes were not exactly positioned, vertical cracks occurred in the semiconductors because the substructure was uneven during sintering.

In an improved experiment, semiconductors were sintered using the so-called “pick and place” process, where semiconductors picked their own sinter-paste from a foil. The sinter-paste was stucked at the bottom side of the semiconductor before positioning at the leadframe. No vertical cracks could be observed at parts where this process was used.

5. Investigation of failed parts

From the data sheet of the IGBT, a differential on-resistance of 2.82 mΩ can be derived. After processing, some failed parts with increased resistances could be observed. As seen in Fig. 5, part 167 showed a forward resistance of 4.11 mΩ and part 54 showed 27.87 mΩ.
To visualize the thermal behavior and to locate areas of higher thermal resistance, lock-in-thermography has been made at part 54, seen in Fig. 6 [10].

The lock-in-frequency was 165 Hz. In the amplitude picture areas of higher thermal resistance (white) can be seen, while in the phase picture, the velocity of the thermal answer is displayed (red). The copper vias of gate and emitter contact are responsible for the limited resolution of Fig. 6, because the thermal conductivity of copper is much higher than that of PCB material.

The lock-in-thermography was able to localize horizontal cracks inside the semiconductor, seen in figure 7.

Fig. 7. Vertical cracks are detected as well, which origin from a mismatch between the position of the IGBT and the position of the sinter paste.

Horizontal cracks are responsible for a lower current carrying capability, however there must be more investigation on understanding the formation of horizontal cracks during production.

However it can be noted, that obviously horizontal cracks do not appear during sintering only, and they do not appear during embedding only. Therefore it is assumed to be the result of both processes together.

A delamination between IGBT and sinter-layer could be observed at part 167, which explains the higher on-resistance, seen in figure 5 (right).

Fig. 5. Output characteristic of failed parts: part 54 (left), 167 (right).

Fig. 6. Lock in thermography: amplitude picture (left), phase picture (right) of part 54. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

Fig. 7. Horizontal and vertical cracked IGBT.

Fig. 8. Measured thermal impedances.

Please cite this article as: R. Randoll, et al., Characteristics and aging of PCB embedded power electronics, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.06.072
6. Thermal impedance

A thermal impedance measurement was done at three different packaging samples of the same IGBTs, see Fig. 8. The construction of the PCB Integrated IGBT is shown in chapter 2. The Al₂O₃ and the AlN samples are IGBTs soldered and bonded on a ceramic substrate as in standard packaging of integrated circuits.

As seen in Fig. 8, the thermal resistance of the PCB integrated IGBT is equal to the standard Al₂O₃ packaging with 0.5 K/W. This low thermal resistance is not only due to the thermal conductivity of the PCB material, but there must be also a substantial heat spreading inside the copper leadframe.

7. Partial discharge investigations

A method to characterize a dielectric material is a partial discharge measurement [5,6].

In application, the partial discharge strength is required to be 3 kV at worst case, especially in the temperature range between $-40 \, ^\circ C$ and $+125 \, ^\circ C$.

A known characteristic of epoxy resin is its decreasing partial discharge (PD) strength at exceeding the glass transition temperature.

Partial discharge measurements have been made at test samples with 150 $\mu$m FR4 material as dielectric. The measurements were made with a 10 kV test equipment. The DUT was immersed in inert liquid to suppress the electrical field. Measurements were made at 1 MHz, with a background noise of 0.5 pC. The AC voltage was ramped up with 0.3 kV/s, until the partial discharge inception voltage set in, then the voltage was ramped further 10% higher, then the voltage was held for 5 s, afterwards the voltage was ramped down at 0.2 kV/s, and the partial discharge extinction voltage was measured as function of the temperature.

The measurement results can be seen in Fig. 9. Applied voltages went up to 6 kV, flowing charges were in the range between 0 and 500 pC.

The measurement (Fig. 9) shows the material capability of 27 kV/mm ($=4 \, kV/150 \, \mu m$) as a constant function of the temperature in the range between 25 and 140 $^\circ C$. Exceeding the glass transition temperature of 150 $^\circ C$, the FR4 material softens, and the partial discharge strength decreases. Since the requirement for the dielectric is 3 kV at worst case, the maximum operating temperature allowed is given by the glass transition temperature minus 25 K margin.

It can be assumed that the PD extinction voltage in the range between 150 $^\circ C$ and the decomposition temperature is constant [5]. The measurement shows that the PCB sample is of good quality, and shows the material properties as expected.

In Fig. 10, the same measurements on different samples were made. Part 3 is a sample of 150 $\mu$m of the same material as in Fig. 9, while part 4 is a sample of 180 $\mu$m of a material with a thermal conductivity of 3 W/mK and a glass transition temperature of 210 $^\circ C$. Therefore the partial discharge extinction voltage stays almost constant up to 170 $^\circ C$, which was the maximum temperature of our test setup.

An increase of the partial discharge extinction voltage to 8 kV at samples with a thickness of 225 $\mu$m could be verified, however with the increase of thickness the thermal resistance increases as well. Measurements dependent on the frequency from 400 kHz to 2.5 MHz showed a constant behavior in this frequency range.

8. Active Power Cycling

One classical lifetime measurement of a power electronic package is power cycling [8,9]. With 17 single IGBT demonstrators, 72000 active power cycling measurements have been made until now without failure. The temperature range was 80 Kelvin, the maximum Temperature was 120$^\circ C$, and the minimum temperature was 40$^\circ C$, the current- on time was 15 seconds as well as the current- off time. No increase of the collector- emitter- voltage could be detected as well there was no increase of the thermal resistance yet. The change in color of one cycled demonstrator is shown in Fig. 11.

9. Aging of PCB material

PCB material is made of epoxy resin, glass reinforcement and ceramic fillers. In case of the tested samples, the fillers are made of Al₂O₃ and MgO, leading to a thermal conductivity of 1.5 W/mK.

Fig. 9. Partial discharge extinction voltage (PDEV) as function of the temperature measured at two samples.

Fig. 10. PDEV versus temperature.

Fig. 11. Color change of a cycled demonstrator.
After stressing 10 samples by 2500 to 3000 temperature shocks from −40 to 125 °C in 30/30 min intervals, all samples showed the same change in color, as shown in Fig. 12.

These aged samples were subjected to partial discharge investigations as well. Hereby, the test voltage started with 2000 V and was increased by 1000 V steps.

In Fig. 13, PD measurements after 2500 temperature shocks can be seen. For 2 samples, after measurement step 7, the dielectric had lost its dielectric behavior.

The interpretation of these measurements is, that the PCB material ages because of the different coefficients of thermal expansion between glass fiber reinforcement and epoxy resin and ceramic fillers. The thermo-mechanical stress is the root cause of losing the PD strength.

In Fig. 14, it can be seen that the temperature shocked and PD stressed PCB material shows delaminations between glass fibers and epoxy resin. At these material interfaces, the thermomechanical stress reaches its maximum.

However it is not yet clear, if this will be the failure mechanism considering the application loads, since the imposed operation voltages are below 500 V.

10. New PCB material

For improving the thermal properties of the construction, new materials are under development. Figs. 15 to 16 show cross sections of such advanced materials. The better thermal conductivity is obtained by increasing the fraction of Al₂O₃ filler in the epoxy.

The interesting thing of this new material is the missing glass fiber reinforcement, which will influence the failure mechanism “conductive anodic filament”.

11. Summary

In this paper the construction of PCB embedded power electronics was described and the challenge of the manufacturing was discussed. The measurement of the thermal impedance shows the substantial heat spreading inside the leadframe and the low thermal resistance of the construction. Partial discharge measurements reflect the PCB material’s dependency on the glass transition temperature (Tg) and demonstrate that application requirements can be reached. Vertical cracks inside the semiconductor have been observed originating from a mismatch between sinter-paste and semiconductor, and can be avoided by the so called “pick and place” sinter process.

The analysis of the galvanic copper layer on top of the semiconductor shows the planarity of the layer and the good resistance during the so called “brown-oxide” etching process during PCB production. An ongoing power cycling measurement has not shown any failure until now. Delaminations between glass fibers and epoxy resin during aging of PCB material by thermal cycling have been demonstrated.

The partial discharge and aging results of this paper show the principle applicability of the PCB embedded technology in power electronic devices.

12. Outlook

The current research work will be continued with leadframe thicknesses of 1 to 1.5 mm, which will increase the effect of the heat spreading. A new PCB material with a thermal conductivity of 7 W/mK and at higher glass transition temperature Tg of 200 °C is in sample production.

These new PCB materials do not have a glass fiber reinforcement, which will influence the failure mechanism “conductive anodic filament” in a positive way.

There is currently research work on a galvanic copper layer with more than 5 μm thickness. Power cycling measurements at test samples are currently running on a test equipment.

The influence of humidity on embedded power electronics will be investigated at Conductive Anodic Filament (CAF) test boards which are already in fabrication.
Acknowledgment

This work has been supported by the German BMBF under contract #16N11654 (Hi-Level) and #01MY12001 (Sphinx)

Lock-in thermography measurements have been acquired on ELITE system from DCG systems, with support of Sector Technologies.

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Please cite this article as: R. Randoll, et al., Characteristics and aging of PCB embedded power electronics, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.06.072