Die crack failure mechanism investigations depending on the time of failure

T. Zirilli
Freescale Semiconducteurs France SAS, Toulouse, France

ARTICLE INFO

Article history:
Received 22 May 2015
Accepted 23 June 2015
Available online xxxx

Keywords:
Die crack
Failure mechanism
Assembly
Root cause investigation
SAM
Fractography
Fault Tree Analysis
Time of failure

ABSTRACT

The quality and reliability concern of the die crack failure mechanism needs to be addressed at each step of the supply chain, from the wafer supplier, semiconductor fabrication, package assembly, Tier1 manufacturer assembly, to the end customer application. Finding the critical factors of a die crack is crucial for the root cause investigation, allowing the implementation of accurate corrective actions. The various analytical methods that can be employed are numerous, from standard FA techniques (mainly SAM & fractography) to advanced techniques like TherMoiré Analysis or Finite Element Simulation. Application-level analysis, problem solving and continuous improvement methodologies are also key success factors for such problems: Fault Tree Analysis and Ishikawa diagram will enable complete process assessment, including package and die integrity, assembly process, Surface-mount technology (SMT) process, and stress condition at the end customer application. This paper first introduces the different and complementary FA techniques, then presents three case studies that illustrate the difficulty to identify the cause of such die cracks, as a function of the time of failure.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

The brittle nature of silicon turns the die into the weakest part of the integrated circuit complex object, in terms of mechanical properties. This is obviously a reliability concern that needs to be addressed at each step of the supply chain, from the wafer supplier, semiconductor fabrication, package assembly, Tier1 manufacturer assembly, to the end customer application. Finding the critical factors of a die crack is crucial for the root cause investigation, allowing the implementation of accurate corrective actions. The various analytical methods that can be employed are numerous [1]. Some die cracks will be easily interpreted and a standard failure analysis (FA) approach will quickly lead to the true cause. But few cases will require extensive application of various FA techniques, and sometimes the expertise of Packaging/Assembly experts.

This paper first introduces the different and complementary FA techniques, then presents three case studies that reflect the difficulty to identify the cause of such die cracks, as a function of the time of failure.

Eventually a discussion about the combination of those methodologies and techniques will take place.

2. Die crack investigation

2.1. Non-destructive techniques

2.1.1. X-ray microscopy

The X-ray microscope is a standard piece of equipment in a FA Lab that uses electromagnetic radiation in the soft X-ray band through the specimen to produce a projected image. It is based on contrast imaging due to the difference in absorption of the sample materials. That principle is a limitation with conventional X-ray absorption technique; poor contrast is obtained when imaging low Z materials and their defects as silicon die cracks. However, that technique is critical to assess the quality of the package itself and to allow validating few assembly parameters (die attach coverage, die placement, etc.), valuable in the crack investigation.

The recent increase of the resolution of the X-ray system and the implementation of 3D X-ray Computed Tomography enables the imaging of such defects without any invasive technique, depending of the dimensions of the die cracks.

2.1.2. Scanning Acoustic Microscopy (SAM)

The SAM uses ultrasound waves to assess the package integrity, evaluating the interfaces between materials. Defects linked to the presence of air such as porosity, voids, cracks or delamination will be obtained, and the package can be approached from every direction.

E-mail address: thomas.zirilli@freescale.com.
The different sample materials have a specific acoustic impedance to be taken into account during the analysis. The nature of a die crack being a fracture of the silicon entails the creation of new interfaces detected by SAM imaging. See Fig. 1 with an example of signal amplitude images obtained on a die corner crack.

2.1.3. Optical profilometry
That non-contact interferometric-based method allows characterizing surface topography. A typical OP analysis provides 2D and 3D images of a surface, roughness statistics, and feature dimensions. It is useful to obtain package surface profile and detect convex or concave warpage.

In Fig. 2, the warpage indicated a thermo-mechanical stress applied to the package during heat excursion of packaging and SMT process.

2.1.4. TherMoiré Analysis or Topography and Deformation Measurement (TDM)
That metrology solution utilizes the shadow Moiré measurement technique to characterize out-of-plane displacement with time-temperature profiling. The sample mechanical behavior can be finely analyzed during a thermal profile. It aims at reproducing real-world processes and operating environments, taking into account the interactions between materials, packages, substrates and complete assemblies. Fig. 3 shows an example of TherMoiré Analysis at the BGA device level.

2.1.5. Electrical fault localization techniques
Few techniques are available to assess the electrical behavior of the faulty devices. In addition to pure electrical measurements (and one can expect parametric or gross functional failures with a die crack), a first information of the spatial location of the die crack itself can be

![Fig. 1. Die corner crack by reflection/transmission.](image1)

![Fig. 2. Contour profile of package: concave warpage.](image2)

![Fig. 3. TherMoiré warpage analysis on a BGA package.](image3)
extracted from specific techniques. Their description is out of the scope of this paper but few can be cited as Time-Domain Reflectometry (TDR), Electro Optical Terahertz Pulsed Reflectometry (EOTPR), Magnetic/SQUID microscopy, and Lock-in Thermography. The benefits of those techniques, already perfectly described in specific publications [2], are that they can be applied without affecting the package integrity, offering more or less a precise location of the physical damage causing the open/short/leakage.

2.2. Invasive techniques

2.2.1. Decapsulation and die extraction from package

That FA step is obvious but is key in the understanding of a die crack. Few of them will be detected only after proper decapsulation and high magnification inspection with an optical/electronic microscope. The use of concentrated acids allows dissolving the upper part of the package or the entire mold compound/leadframe. With the bare die, the investigations will be done on the front side, back side and edges of the die. Fig. 4 shows a linear crack that was not detected by standard non-destructive techniques.

2.2.2. InfraRed (IR) confocal microscopy

An IR laser confocal microscope allows investigating silicon die cracks from the front side or the back side. Silicon semiconductor is almost transparent to IR radiation (high optical transmission). As opposed to perfect transmission through the silicon crystal, light scattering will occur at anomalies like delamination or cracks. Those light scattering centers can be easily identified, like in Fig. 5 example.

2.2.3. Cross-sectional study

That method can be used to assess the package quality, most of the time consequently to validate a failure mechanism after X-ray/SAM inspections. The sample can be prepared with mechanical cross-section, ion milling, standard/Laser/Plasma FIB, pending the area to be analyzed and the required surface polishing quality. The artifacts linked to the cross-section itself towards the presence of cracks in the sample should be closely monitored and not lead to misinterpretation. That analysis can be performed at system, PCB or device level and will provide a lot of valuable information for the die crack investigation. Fig. 6 displays a severe die crack linked to a mold compound/leadframe delamination.
2.2.4. Fractography

This is one of the key techniques, a must-do for the die crack investigation. Fracture surfaces are produced when silicon breaks and can be observed with optical/electronic microscopy. The appearance of the surface, particularly the topography, depends on the conditions under which it was broken. Many references described thoroughly the different patterns [3]. The fractography describes the ways of studying these surfaces, based on the fracture patterns. Those are the most typical terms used to describe specific topographical features:

- Wallner lines, bowed in the direction of crack travel.
- River lines converge in the direction of crack travel.
- Mirror region, smooth, around the nucleus region.

Fig. 7 shows a side and back side view of a broken die due to a visible mechanical impact (die ejector). Note the 'mirror region' around the initial crack, and the visible propagating fracture wavefront.

The brittle fracture theory applies to silicon and offers various types of information on the cracks: origin, velocity and direction of crack travel.

2.3. Investigation methodology

On complex cases, in addition to the first FA results using the discussed techniques, additional pieces of information need to be gathered in an organized fashion to understand the failure origin.

2.3.1. Thought processes

Fault Tree Analysis (FTA) and Ishikawa diagrams are useful to thoroughly review any potential cause during the manufacturing/assembly/customer assembly processes, considering each factor: man, material, method, machine and environment.

Failure anamnesis [4], diagnosis consisting in considering the problem from a system/application standpoint instead of device-level, will also help in revealing hidden root causes that can be attributed to the application itself. That critical piece of information cannot sometimes be extracted from device-only-related FA. In addition, cost and time avoidance is enabled through asking the right questions before the actual failure analysis work with complex and expensive techniques.

2.3.2. Failure reproduction

Then to verify a failure scenario, two other technical means can be applied.

Mechanical simulation with Finite Element Simulation is a powerful tool to address die crack issues, quantifying the impact of each parameter [5] but also to anticipate risky situations like over-height die attach fillet, as shown in Fig. 8 [6].

Die crack replication (with die bend test like Fig. 9 or ball breaker method) can be used to quantify the silicon die strength and compare the fracture with known cases.

Those methods are employed to develop new product packages as well as to implement corrective actions facing fractured dice.

3. Die crack case studies

Three automotive IC examples are described in that section. The supply chain until the end customer for a semiconductor device in a car includes suppliers, Foundry, Tier1 manufacturer and OEM car manufacturer. The electrical failures caused by a die crack can appear at various stages of the product life. The time of failure hence will be an indicator on how the FA can be conducted.

3.1. Tier1 manufacturer — line pull

Over the courses of few weeks, recurring issues were observed with an injection driver product (LQFP64) on multiple date codes, returned as Line Pull rejects. Several failure modes were present but all failures were due to silicon die cracks. FA revealed rapidly, using decapsulation, optical inspection and die fractography, that the die crack started from the back side and propagated to the top, starting from a surface point damage (Fig. 10).

Those impact points (Fig. 11) clearly were the nucleation site of the crack, propagating from those points. They were most likely the cause of the mechanical weakness of the devices, revealed by the Tier1 manufacturer reflow process.

As a consequence a complete review of all manufacturing and assembly steps was conducted: Lot history, Assembly process and Tool commonality were cross-checked with all the data from the return cases. It showed few common steps on the affected lots. Then a FTA was carried out for the die back side point damage on the processes of backgrind, delaminate, inking, clean, bake, inspection, shipping, etc. Potential causes were verified and led to a consistent failure scenario: silicon particles from the backgrind process were not completely removed by the cleaning process. Those particles were transferred from the wafer backside to the equipment, causing point damage during subsequent
Fractography revealed a similar pattern. A cross-sectional study was also carried out to validate the assembly manufacturer process on that braking valve driver (TQFP128). ICs were analyzed with decapsulation, optical inspection and die fractography. A mapping was done using the suspected equipment overlay with the die crack wafer locations. The particles were quickly confirmed on the ink equipment plastic handler, allowing specific corrective actions. That example shows that on recurring die cracks with a similar pattern captured early in a Tier1 manufacturer process, the IC supplier can be suspected and causes should be explored in its Manufacturing/Assembly plants. In that case the thermo-mechanical stress of the SMT process was the trigger event for the crack.

3.2. OEM car manufacturer — 0 km reject

Single digit cases were found defective early in the OEM car manufacturer process on that braking valve driver (TQFP128). ICs were first analyzed with decapsulation, optical inspection and die fractography. A cross-sectional study was also carried out to validate the assembly process quality. Severe die cracks were observed, as shown in Fig. 12.

Based on such crack patterns (Fig. 13) and internal investigations (Fault Tree Analysis, Ishikawa diagram), one suspects that the root cause is due to external package stress. It was likely to occur after electrical test as these parts had passed ATE initially.

Given that no suspicion was lying on the IC supplier, the Tier1 manufacturer also carried out a root cause analysis exercise at PCB and system level. Topography and Deformation Measurement technique was even employed but could not explain such a catastrophic failure. It was concluded that the units were delivered according to their specification and must have been damaged afterwards. As a consequence, the Hydraulic Electronic Control Unit was carefully inspected: small dents and scratches indicated that the units have been dropped (see Fig. 14). Due to its considerable weight, the impact applied a high peak of mechanical stress via the ECU and the PCB to the IC mounted on the heatsink.

A drop test was performed to confirm that hypothesis and was a successful failure reproduction. That example demonstrated that isolated cases with catastrophic damages captured at OEM car manufacturer were most likely not due to the IC supplier. Quick FA validation of the original assembly quality enabled focusing more on PCB or system level, with different investigation techniques.

Various analytical methods were employed in addition to the standard FA techniques to move forward with the root cause investigation. Four point bend test was used to assess the die flexural strength from chips of the standard production flow. The die break failure mode with a lower die strength correlated with the actual die crack situation (Fig. 16). It can be concluded that the lower die mechanical strength could be one contributing factor to the die crack issue.

Various production parameters were evaluated and optimized to have a more robust silicon (dicing saw process, SEZ wafer etching after backgrinding ...). But a key indication of the TherMoiré Analysis and digital modeling was that the root cause of the die cracks was also attributed to the SMT process and PCB board design inducing high thermo-mechanical stress onto the package. TherMoiré Analysis on two different PCB designs indicated that the full flag solder pad design generated less stress than 4 solder bar solder pad design with a significant package warpage reduction (Fig. 17).

4. Conclusion

4.1. Discussion

This paper is explicitly showing the many ways to characterize a die crack issue. A lot of factors are to be considered when attempting to establish a FA flow pending the time of failure and other parameters like event occurrence quantity for instance. A proposed flow is visible in Fig. 18.

That decision tree is based on few principles that the analyst should bear in mind. First is that a die crack results in electrical malfunction that will be tested all along the supply chain process. Hence the probability to obtain field failures with an IC issue only is lower than the line failures, probably revealed by the Tier1 manufacturer assembly reflow. Second, the quantity of returns is also an interesting indicator of the problem nature: unique or systemic. The FA approach will naturally be more developed in that last case and will require methodology as well as various techniques to conclude. Third, the understanding of the system conditions when the failure appeared is key to determine the true root causes.

3.3. End customer reject — field failure

There were multiple die crack incidents reported on SOIC54 exposed pad packages from one SMT customer [7]. FA investigations gathered a lot of information on the different line & field failures, see Fig. 15. The fractography revealed a similar pattern.
Fig. 14. Application module with mechanical damage signs.

Fig. 15. Die crack mapping with the package outline.

Fig. 16. Die break failure modes with 4 point bend test.

Fig. 17. Stressful PCB design and TherMoiré Analysis.
Silicon die crack is a common failure mechanism and reliability concern to be addressed at each step of the supply chain, from the wafer supplier, semiconductor fabrication, package assembly, Tier1 manufacturer assembly, to the end customer application. Finding the critical factors of a die crack is crucial for the root cause investigation, allowing the implementation of accurate corrective actions. The various analytical methods that can be employed are numerous, from standard FA techniques (mainly SAM & fractography) to advanced techniques like TherMoiré Analysis or Finite Element Simulation.

This paper introduced different and complementary FA techniques. Then three case studies at different times of failure showed the complexity of those analyses and the most efficient ways to approach the global root cause investigation.

Acknowledgments

The author would like to express his thanks to the Toulouse FA Lab personnel as well as to the Freescale worldwide package experts.

References