Visualization of gate-bias dependent carrier distribution in SiC power-MOSFET using super-higher-order scanning nonlinear dielectric microscopy

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1. Introduction

Silicon carbide (SiC) is an attractive material for power semiconductor devices especially in high voltage application area [1]. Although SiC power devices are now practically in use, further research and development (R&D) for enhancing their electrical performance, reliability, and cost reduction are required. Techniques for evaluating device structure including activated carrier distribution are required for effective R&D.

Previously, we have reported that scanning nonlinear dielectric microscopy (SNDM) [2] and its extended method, super-higher-order SNDM (SHO-SNDM) [3], are powerful tools for visualizing carrier distribution in cross-section of SiC devices. However, previous measurements were performed to non-operated device. Carrier profiling of operated device provides insight to the physical origin of electrical characteristics in actual device. Although such analysis for Si transistors using scanning capacitance microscopy (SCM) has been already performed [4], carrier profiling of operated SiC device has not been reported. The reason is considered to be the difficulty of carrier profiling of SiC devices caused by small capacitance response to the voltage [5], which degrades signal-to-noise ratio of SCM measurement.

In this study, carrier distribution of cross-sectioned operated SiC power MOSFET was measured. At first, “on” and “off” states were measured in detail using SHO-SNDM and variation of depletion layer distribution was visualized (experiment 1). Second, carrier distribution as a function of gate-source voltage \( V_{GS} \) was measured in detail (experiment 2).

2. Principle

2.1. SNDM

SNDM is one of the types of scanning probe microscopy (SPM) which measures capacitance \( C_1 \) response to the applied voltage between metal-coated tip and sample. The resulting image of SNDM measurement is 2D mapping of \( \partial C_1 / \partial V \) which can be interpreted to carrier distribution. The basic principle is illustrated in Fig. 1(a). The capacitance sensor of SNDM (SNDM probe) consists of free-running RF LC oscillator to which a metal-coated cantilever tip is attached. In this paper, the oscillating frequency is ~4 GHz. When the tip is contacted to the sample surface, the oscillating frequency of SNDM probe is determined by tip-sample capacitance \( C_s \) and built-in capacitance \( C_0 \) and built-in inductance \( L \). The \( C_s \) varies and oscillating frequency is modulated, when external voltage with amplitude of \( V_{GS} \) and an angular frequency of \( \omega_0 \) is applied between tip and sample. The original capacitance variation is obtained using frequency demodulator. As external voltage \( V_S(t) \) is described by

\[
V_S(t) = V_{S,0} \cos \omega_0 t, \tag{1}
\]

the capacitance variation can be given by the following Fourier expansion form

\[
\Delta C_1(t) = \sum_{n=1}^{\infty} \left( C_n^\cos \cos n \omega_0 t + C_n^\sin \sin n \omega_0 t \right). \tag{2}
\]

Coefficients in Eq. (2) can be extracted from frequency demodulator output by using multi-channel lock-in amplifier.

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When $V_{GS,0}$ is small, $C_{1co} = V_{GS,0}(\partial C_s/\partial V|_{V=0})$ then $\partial C_s/\partial V|_{V=0}$ image can be obtained by measuring the fundamental harmonic component in the frequency demodulator output.

2.2. SHO-SNDM

2.2.1. Capacitance-voltage curve reconstruction

By obtaining all harmonic components and using both of Eqs. (1) and (2), capacitance-voltage (C-V) curve is reconstructed at each pixel [3], which enables further sophisticated analysis such as depletion layer visualization [3] which was performed in experiment 1. The C-V curve reconstruction can be performed by the following steps: At first, acquired data and amplitude of applied voltage are substituted to curve reconstruction discussed in Section 2.2.1, full $\partial C_s/\partial V|_{V=0}$ image can be obtained at once from Eqs. (3) and (4) [6].

$$\partial C_s/\partial V(t) = \alpha_0 + \sum_{n=1}^{\infty} (\alpha_n \cos n\omega_0 t + \beta_n \sin n\omega_0 t).$$

The coefficient $\alpha_0$ is time-averaged $\partial C_s/\partial V|_{V=0}$ signal. The coefficients $\alpha_n$ and $\beta_n$ are extracted from time dependent $\partial C_s/\partial V|_{V=0}$ signal (detail of setup will be shown in Section 3.2). Using the same concept with the C-V curve reconstruction discussed in Section 2.2.1, full $\partial C_s/\partial V|_{V=0}$ VS $V_{GS,0}$ relation in the gate voltage range of $V_{GS,0} < V_{GS} < V_{CS}$ can be obtained at once from Eqs. (3) and (4) [6].

3. Experimental

3.1. Sample detail

Cross-section of a commercially available SiC power MOSFET whose nominal threshold gate voltage is 2 V was mechanically and chemically polished. Thin conductive wires were pasted to electrode pads on the device surface with silver paste in order to apply operating bias voltage. The device function was confirmed after sample preparation by checking that the drain-source resistance is changed by $V_{GS}$.

3.2. Experimental setup

Fig. 2 illustrates the experimental setup employed for our measurements in this study. For modulating $C_1$, an ac voltage with amplitude of $V_{S,0}$ and angular frequency of $\omega_0$ was applied between tip and sample, which induces the frequency modulation of SNDM probe output [2]. The SNDM probe output is demodulated followed by extraction of $C_{1co}$ and $C_{1co}$ using lock-in amplifier L1 (experiment 1). For measuring $V_{GS}$ dependence of $\partial C_s/\partial V$, $\alpha_0$ and $\beta_n$ are extracted from $C_{1co}$ signal using lock-in amplifier L2 and LPF (experiment 2).

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For driving the gate, an ac voltage source ($V_{GS,ac}$) and a dc voltage source ($V_{GS,dc}$) are connected in series and then to the sample, while the drain and source are shorted. Application of $V_{GS}$ can induce a tip-sample potential difference, which causes an unexpected modulation of SNDM signal resulting in artifact on SNDM image. To avoid this artifact, unlike regular SNDM/SHO-SNDM setup, some extra components were added in the setup: a piezo actuator on the SNDM probe and tip-sample voltage canceller (the basic concept is same as Kelvin probe force microscopy but extended for canceling ac potential). Prior to SNDM measurement, tip-sample voltage cancelation procedure was performed at every measurement point as follows: the cantilever tip was retracted up to ~50 nm from the sample surface and excited at frequency slightly above the mechanical resonance frequency (~70 kHz). And then tip-sample ac voltage $V_{ac}(t) = V_{ac0} \cos \omega t$ was applied. The vibration amplitude of cantilever and its variation which synchronizes with $V_{ac}(t)$ are detected by lock-in amplifiers LI3 and LI4. The output of LI4, which is proportional to tip-sample potential difference, is used for tip-sample voltage cancelation. All the components were linked together and controlled by a computer.

3.3. Experimental conditions

All measurements were performed in air at room temperature. In experiment 1, only dc voltages were applied to gate-source. $V_{GS,dc} = 0$ V and 5 V for “off” and “on” state, respectively. In experiment 2, gate was biased only with an ac voltage to the source. The amplitude and frequency were 4.5 V and 120 Hz, respectively.

4. Results and discussions

4.1. Experiment 1

Up to the 4th order harmonic images were obtained and used to depletion layer distribution analysis [3] as briefly explained as follows: local C-V curve is reconstructed and categorized to monotonously increasing curve, monotonously decreasing curve and V-shape curve, which correspond to p-type, n-type and depletion region, respectively [6]. The analytical results are shown in Fig. 3(a) and (b). The p-, n-, and depletion areas are distinguished by three colors: white, black, and brown, respectively. Fig. 3(a) and (b) are for “off” state and “on” state, respectively. In Fig. 3(a), n-drift area and n-source area are colored with black, which means that they were determined to be n-type area. The p-body was surely determined to be p-type and colored with white. The gate was also determined to be p-type. The area under the gate is determined to be depletion area, where no electron channel is formed. In contrast, in Fig. 3(b), depletion area under the gate almost disappeared and n-type region was expanded directly under the gate. In addition, between the gate and p-body, n-type path which connects n-drift area and n-source area appeared. This means that electron channel was formed. On the other hand, white colored area (p-area) was a little shrunk, because holes were repulsed from the positively biased gate. As shown here, distributions of carrier and depletion region in “off” and “on” states were reasonably visualized.

4.2. Experiment 2

Unlike experiment 1, depletion region analysis is not performed but the $V_{GS}$ dependence of carrier distribution is analyzed in detail. Fig. 4(a) shows the area where it was scanned in this study. Up to the 6th order harmonic images were obtained (not shown) and substituted to Eq. (4) followed by full relation analysis of $V_{GS}$ vs. $\partial C_s/\partial V_{GS} |_{V_{GS}=0}$, which enables reconstruction of $\partial C_s/\partial V_{GS} |_{V_{GS}=0}$ images at arbitrary $V_{GS}$. For instance, Fig. 4(b)–(d) shows reconstructed images for $V_{GS} = -1.98$ V, 1.53 V, and 4.41 V, respectively. Positive $\partial C_s/\partial V_{GS} |_{V_{GS}=0}$ and negative $\partial C_s/\partial V_{GS} |_{V_{GS}=0}$ mean p-type and n-type, respectively. In these images, the gate is displayed as weak positive signal ~10 mV. In Fig. 4(b), p-body and
n-type area exhibit strong positive signal ~300 mV and negative one ~−100 mV, which are out of color range. The color range is adjusted to show the changes directly under the gate (as a result, p-body and n-type area looks saturated). When \( V_{GS} \) is negative (Fig. 4(b)), electrons are fully exhausted from the area under the gate and the \( \partial C_s/\partial V|_{V=0} \) signal is almost zero. Positive \( V_{GS} \) attracts the electrons and n-type region expands toward the gate, which is observed in Fig. 4(c). Further increase of \( V_{GS} \) causes the electron accumulation and inverse layer (i.e., channel) formation under the gate, which is visualized in Fig. 4(d).

These changes in \( \partial C_s/\partial V|_{V=0} \) images agree with the principle of n-channel MOSFET operation; positive gate voltage accumulates electrons in n-type region under the gate and forms inversion layer in p-type region, which becomes electron channel between n-drift area and n-source area. We have to point out the discrepancy between nominal threshold gate voltage (2 V) and the voltage at which channel formation was observed (over 4 V). This can be attributed to the electron field decay due to fringe effect caused by cross-sectioning of device. Therefore, simulation is needed for direct comparison of the measurement result and realized device characteristic. On the other hand, even if simulation cannot be performed, comparison between failure device cell and good device cell can be possible.

5. Summary

Carrier distribution of an operated SiC power MOSFET was measured by SHO-SNDM. In experiment 1, depletion layer re-distribution under the “off” and “on” state was visualized. In experiment 2, detailed \( V_{GS} \) dependence of carrier distribution was also visualized. These results show the capability of SHO-SNDM for evaluating operated SiC devices. Although numerical simulation might be needed to qualitative evaluation, these techniques discussed here is applicable to comparison between failure and good device.

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