Impacts of plasma process-induced damage on MOSFET parameter variability and reliability

Koji Eriguchi*, Kouichi Ono

Graduate School of Engineering, Kyoto University, Kyoto-daigaku Katsura, Nisikyo-ku, Kyoto 615-8540, Japan

ARTICLE INFO

Article history:
Received 25 June 2015
Received in revised form 30 June 2015
Accepted 1 July 2015
Available online xxx

Keywords:
Plasma-induced damage
MOSFET
Variability
Threshold voltage
Drain current
TDDB

ABSTRACT

Plasma process-Induced Damage (PID) is one of the critical issues in designing Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs), because PID is believed to enhance reliability degradation and the variability. This paper presents how PID impacts on the variability and reliability characterization by focusing on two key damage creation mechanisms, i.e., Plasma-induced Physical Damage (PPD) and Charging Damage (PCD). In PPD mechanisms, the effects of Si loss in the source/drain extension region and latent defects on MOSFET performance are discussed by means of the PPD range theory and Technology-Computer-Aided-Design (TCAD) simulations. It is presented that, under the fluctuation of plasma parameters, PPD enhances variability of threshold voltage shift ($\Delta V_{th}$) and drain current. Regarding PCD mechanisms, $\Delta V_{th}$ variation due to high-k dielectric damage is investigated by reviewing an antenna ratio distribution reported so far. Finally, two key concerns are discussed as future perspective—PPD on a fin-structured FET and PCD on high-k Time-Dependent Dielectric Breakdown (TDDB) characterization. Since PID is the intrinsic nature of plasma processing, variability enhancement and reliability degradation by PID should be taken into account for future Very-Large-Integration (VLSI) circuit designs.

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1. Introduction

Plasma process-Induced Damage (PID) is of great importance in designing Very-Large-Scale Integration (VLSI) circuit and the modern manufacturing processes [1,2]. In general, PID is classified on the basis of mechanisms such as charging damage, physical damage, and radiation damage [2]. For example, Plasma-induced Physical Damage (PPD) is induced by high-energy ion bombardment incident on Si or other material surfaces [3,4]. This damage creates defects (such as Si vacancies, displaced Si atoms, interstitials and dangling bonds) and forms, as a consequence, the damaged layer in a Si substrate and remaining localized defects underneath the layer [5]. One of the key practical problems respective to PPD is “Si recess” [6,7]—removal of the damaged layer by a subsequent wet-stripping step results in a recess structure in the Source/Drain (S/D) extension regions of Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) [8]. This damage structure induces threshold voltage shift ($\Delta V_{th}$) [8] and the remaining defects after the wet-stripping step lead to a drain current ($I_d$) decrease [9]. Plasma-induced Charging Damage (PCD) is induced by conduction current from plasma flowing into gate dielectrics, resulting in the degradation of MOSFET reliability [10–12]. In general, there are two types of PCD, i.e., continuous current flowing into the gate dielectrics in accordance with an applied bias waveform and an electrostatic-discharge-like temporal charge injection occurred during de-chucking of wafers or at the edge of wafers during the process. PCD is often associated with the antenna effect [13], caused by the collection of charges by an electrically floating metal interconnect connected to the gate electrode. The antenna ratio $r$ (=exposed metal interconnect area/gate area) is generally used as a measure of PCD. The antenna effect is enhanced by the length of interconnects, i.e., the damage (usually quantified by $\Delta V_{th}$) is enhanced with increasing $r$. Historically, from the viewpoint of device technology, PCD has been investigated using not only bulk Si but also SOI devices [14]. Regarding gate dielectric materials, PCD has been a critical (reliability) problem, particularly for high-k dielectrics [15–17], which are sensitive to charge trapping mechanism. It was reported [17] that, owing to this characteristic trapping mechanism, PCD induces $V_{th}$-instability of a MOSFET. Fig. 1 summarizes these PID mechanisms.

Regarding the state-of-the-art VLSI circuit designs, the parameter variation of MOSFETs such as $V_{th}$ variability has become a crucial problem [18,19]. The parameter variation is believed to significantly impact on not only VLSI performance design but also the reliability characterization such as Negative Bias Temperature Instability (NBTI) tests [19,20]. Therefore, it is expected that the variation induced by PPD and PCD (e.g., $\Delta V_{th}$ and $I_d$) should be comprehensively clarified to ensure reliability of MOSFETs where the parameters are used as the principal measures. To realize accurate characterization schemes, it is extremely important to develop plasma-induced $V_{th}$ and $I_d$ variability models. In this paper, we present comprehensive PID-enhanced variability models being linked to reliability prediction, and investigate how each PID

* Corresponding author.

E-mail address: eriguchi@kuaero.kyoto-u.ac.jp (K. Eriguchi).

http://dx.doi.org/10.1016/j.microrel.2015.07.004

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Please cite this article as: K. Eriguchi, K. Ono, Impacts of plasma process-induced damage on MOSFET parameter variability and reliability, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.07.004
mechanism impacts on the parameter variation in a VLSI circuit, in particular, for reliability assessment where $\Delta V_{th}$-variation is critical\[19,20\]. Future key issues imposed by PID in ultimately-scaled regimes are also discussed.

2. Experimental and simulation schemes

Two types of test structures were used in this study. For PPD study, n-type (100) Si substrates with a resistivity of 0.02 $\Omega$ cm were exposed to Ar plasma generated in an Inductively Coupled Plasma (ICP) reactor for 30 s. The source ICP power was 300 W and the pressure was 2.7 Pa. An RF bias at 13.56 MHz was applied to a wafer stage with powers ranging from 25 to 150 W. Plasma diagnostics using a Langmuir probe and an oscilloscope determined the average self dc bias ($V_{dc} < 0$) and the plasma potential ($V_p = 11$ V). (The electron temperature was estimated to be 2.7 eV.) Thus, the average energy of incident ions $E_{ion}$ is defined as $V_p - V_{dc}$. $E_{ion}$ is used as a measure for PPD discussion.

For PCD study, MOSFETs with a high-k stack film (6.4-nm-thick HfAlO$_x$/1.5-nm-thick interfacial SiO$_2$) were fabricated and exposed to Ar plasma in a Capacitively Coupled Plasma (CCP) reactor. Bias power applied to a wafer stage was 20 W. In this case, $V_{dc}$ was estimated to be $\sim 350$ V from the oscilloscope monitoring. The bias frequency was 13.56 MHz. The electron temperature was estimated to be $\sim 4.0$ eV. Details of the sample structure were described elsewhere\[21–23\]. Al probing pads with a constant area of 42000 $\mu$m$^2$ served as antennas of the box-type structure. For $V_{th}$ analysis, MOSFETs with channel length = 2 $\mu$m and width = 1 $\mu$m were evaluated. For Constant-Voltage Stress (CVS) and Constant-Current Stress (CCS) Time-Dependent Dielectric Breakdown (TDDB) measurements, MOS capacitors with an area of 10000 $\mu$m$^2$ were evaluated. For each wafer, the measurements were carried out for at least fifteen different devices to evaluate the deviation.

Most of the results provided in this paper are obtained from simulations. To perform a model prediction of the parameter variation induced by PID, we employed the PPD range theory\[22\], Technology-Computer-Aided-Design (TCAD)\[24\], and Molecular Dynamics (MD) simulations\[25\]. In the TCAD simulations, a drift–diffusion-based model was employed to simulate drain current–gate voltage characteristics. The geometrically recessed structure and defect density were introduced in the damaged devices. In the MD simulations, a classical Newtonian equation of motion was solved using interatomic potential model provided by Ohta et al.\[26\]. Details of these simulation schemes are reported elsewhere\[8,9,22,25,27\]. To estimate variations, more than $10^6$ devices are evaluated by using a Monte Carlo method.

3. Results and discussion

3.1. $\Delta V_{th}$-variation by PPD

Fig. 2 shows the damaged layer thickness ($d_{dam}$) as a function of ($V_p - V_{dc}$) corresponding to the average ion energy $E_{ion}$ under the ICP exposure. The thickness was determined by spectroscopic ellipsometry with an optimized optical model\[28\]. The damaged layer in this case is assumed to consist of Surface Oxidized (SL) and Interfacial Layers (IL) with localized defects\[28,29\]. As seen, the power-law dependence is obtained, which is expressed as,

$$d_{dam} = A_{PPD} \cdot \left(\frac{E_{ion}}{V_p - V_{dc}}\right)^{\alpha}$$

(1)

where $A_{PPD}$ and $\alpha$ are process- and material-dependent parameters. (In this case, $A_{PPD} = 2.2$ and $\alpha = 0.19$.) Note that this dependence can be verified by the PPD range theory\[22\]. Under a given defect profile, a

![Fig. 1. During plasma exposure, devices are damaged by bombardment of high-energy ions and plasma stressing current flowing into high-k dielectric films enhanced by the so-called antenna effect. These mechanisms are usually referred to as Plasma-induced Physical Damage (PPD) and Charging Damage (PCD), respectively.](image1)

![Fig. 2. Dependence of damaged layer thickness on the average ion energy. The thickness was determined by spectroscopic ellipsometry.](image2)

Please cite this article as: K. Eriguchi, K. Ono, Impacts of plasma process-induced damage on MOSFET parameter variability and reliability, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.07.004
recess depth is then determined with respect to a wet etch process condition. By using the PPD range theory again, one can estimate the recess depth \( d_R \) as a function of \( E_{\text{ion}} \) for various wet-etch conditions [30] as indicated in Fig. 3. Hence, the relationship between \( d_R \) and \( E_{\text{ion}} \) is written as

\[
d_R = B_{\text{PPD}} \cdot (E_{\text{ion}})^\beta,
\]

where \( B_{\text{PPD}} \) and \( \beta \) are process- and material-dependent parameters. (In Fig. 3, \( B_{\text{PPD}} \) and \( \beta \) are 0.92 and 0.32 for the low bias frequency limit, respectively, and 0.83 and 0.31 for the high bias frequency limit, respectively.)

Formation of recess structure primarily induces \( V_{\text{th}} \) shift [8]. Since \( \Delta V_{\text{th}} \) is found to be in proportion to \( d_R \) from TCAD simulations and an analytical device model [8], the dependence of \( \Delta V_{\text{th}} \) on \( E_{\text{ion}} \) is described as

\[
\Delta V_{\text{th}} = -B_K \cdot (E_{\text{ion}})^\beta,
\]

where \( B_K \) is a process-dependent parameter. In the following discussion, we set \( B_K \) and \( \beta \) to 10 mV and 0.3, respectively, based on the results in Fig. 3 and TCAD simulations.

When \( E_{\text{ion}} \) or an Ion Energy Distribution Function (IEDF) varies in response to “fluctuation of plasma” during etching, \( \Delta V_{\text{th}} \) of damaged MOSFETs in a VLSI has a certain distribution. Now we can predict the distribution by using Eq. (3). We assume the standard deviations of incident ion energy in the IEDF to be 3% of \( E_{\text{ion}} \). Fig. 4a shows the estimated \( \Delta V_{\text{th}} \) distribution for \( >10^6 \) devices for \( E_{\text{ion}} = 50 \), 100, and 200 eV. As seen, the variability of \( \Delta V_{\text{th}} \) is enhanced by increasing \( E_{\text{ion}} \). (The increment along the x-axis is 0.05 mV.) Fig. 4b shows the standard deviation as a function of \( E_{\text{ion}} \). Overall the standard deviation \( \sigma \) becomes ~0.3 mV, giving \( 3\sigma = -1 \) mV. This may be negligible, compared with \( V_{\text{th}} \) variability in literatures [20,31] and the results for PCD case discussed later in this paper. However, in this case, the variation of \( d_R \) corresponds to ~0.1 nm, equivalent to the distance between each atomic plane in the single crystalline Si structure [30]. This implies that the obtained variation is intrinsic and inevitable, regardless of process technology.

### 3.2. Drain current variation by PPD

In present-day manufacturing processes, the damaged layer is stripped off by a wet etch step with a designed criterion. However, as pointed out in literatures [32–34], the generated defects are difficult to remove completely by applying conventional wet-etch and annealing processes. Even if a long-time wet-etch step is applied, there still remains the latent defect in the damaged Si region. The dependence of the density \( n_{\text{dam}} \) is generally expressed as

\[
n_{\text{dam}} = C_{\text{PPD}} \cdot (E_{\text{ion}})^\gamma,
\]

where \( C_{\text{PPD}} \) and \( \gamma \) are process- and material-dependent parameters [30]. Fig. 5a shows defect density as a function of \( (V_p - V_{\text{th}}) \) experimentally obtained using n-type Si(100) substrates. \( C_{\text{PPD}} \) and \( \gamma \) are \( 6.8 \times 10^{15} \text{ cm}^{-2} \) and 1.7, respectively, in Fig. 5a). The density was determined by a capacitance–voltage method proposed previously [29]. In estimation of defect density, the thicknesses of SL and IL obtained by spectroscopic ellipsometry were considered. The observed power-law dependence is in consistent with Eq. (4). Note that the density range is on the order of \( 10^{18} \)–\( 10^{19} \text{ cm}^{-2} \), which is in good agreement with MD simulation results [29]. Thus, these remaining defects decrease drain current of the damaged device \( (I_{\text{dam}}) \). Since \( I_{\text{dam}} \) depends linearly on \( n_{\text{dam}} \) [8], the dependence of \( I_{\text{dam}} \) on \( E_{\text{ion}} \) is written as

\[
I_{\text{dam}} = I_0 \cdot (1 - D_{\text{dam}} \cdot E_{\text{ion}})^\gamma,
\]

where \( I_0 \) is drain current without PPD and \( D_{\text{dam}} \) is a device-dependent parameter. Fig. 5b shows \( I_{\text{dam}} \) degradation derived from 65-nm-technology-based TCAD simulations with experimental data. \( D_{\text{dam}} \) is
1.6 × 10^{-5}, in this case.) The standard deviation as a function of $E_{\text{ion}}$ is also displayed. As seen, the standard deviation becomes ~0.3% of $I_0$, giving $3\sigma = -1\%$ of $I_0$. This may not be negligible in a VLSI circuit design.

3.3. $\Delta V_{\text{th}}$-variation by PCD

Fig. 6a shows $|\Delta V_{\text{th}}|$ as a function of $r$ for various MOSFETs damaged by two process times, i.e., 30 and 120 s ($\Delta V_{\text{th}} < 0$). As seen, the power-law relationship

$$|\Delta V_{\text{th}}| = E_{\text{PCD}} \cdot r^\eta$$

is confirmed in the present $r$-range, where $E_{\text{PCD}}$ and $\eta$ are process- and device-dependent parameters, respectively. (In Fig. 6a, $E_{\text{PCD}}$ and $\eta$ are 5.0 and 0.21 for 30-s plasma exposure, respectively, and 22.0 and 0.22 for 120-s plasma exposure, respectively.) In present-day VLSI circuits, the length of interconnect tied to each MOSFET is optimized in accordance with chip performance as well as the antenna design rule [35–38]. Therefore, the antenna ratio $r$ itself varies—within the antenna design rule—from device to device in the circuit where billions of MOSFETs are built-in. Note that the representative interconnect length distribution in a VLSI circuit is called Rent’s rule [39,40]. A model prediction was performed previously when the antenna ratio $r$ obeys Rent’s rule [41]. Here in this study, we employ an $r$-distribution obtained from literatures [35,36] as shown in Fig. 6b. We introduce this practical antenna ratio distribution function $f(r)$ which is analytically expressed as

$$f(r) = r^{-3}$$

in the range of $r > 10$. (Note that $f(r)$ should be normalized for variability prediction with respect to $r$.) We set $E_{\text{PCD}}$—charging parameter—to be 5, 10, and 20 mV as typical PCD for the purpose of simplicity in the following discussions. The calculated $\Delta V_{\text{th}}$ distributions based on $f(r)$ from the literature for various $E_{\text{PCD}}$ are shown in Fig. 7a (The increment along the x-axis is 2 mV), and the standard deviation as a function of $E_{\text{PCD}}$ for various $r$ in Fig. 7b. In contrast to PPD presented in Fig. 2b, the $\sigma(\Delta V_{\text{th}})$ by PCD becomes significant amount, i.e., enhancement of $\Delta V_{\text{th}}$ becomes comparable to widely-discussed $V_{\text{th}}$ variability attributed to Line-Edge-Roughness (LER) [42], Line-Width-Roughness (LWR) [43], and dopant fluctuation [44]. As suggested in Eq. (6), the charging parameter should be decreased to suppress PCD itself as well as the $\Delta V_{\text{th}}$ variation.

3.4. Future perspective of PID

Recently, the mass production of three-dimensional (3D) fin-type FETs—double-gate or trigate FETs called finFETs—has been realized [45,46]. Both lateral straggling of incident ions and bombardment of sputtered species are believed to be fundamental mechanisms for defect
creation in the fin (sidewall) during finFET etching\cite{47,48} as shown in Fig. 8. Formation of damaged layer in the vertical and lateral directions in the fin bulk may result in remaining defects after a wet-etch process. However, in the following wet-etch step, a criterion for the removal thickness is determined uniquely by the number of defects. This process constraint results in a serious problem—remaining defect density becomes almost the same with each other regardless of the directions, i.e., only the recess depths are different. Therefore, although “as-created” defects in the sidewall is considered to be small in number due to the nature of PPD creation mechanism, the number of latent defects at the sidewall becomes comparable to those along the vertical axis, implying that finFETs may suffer from PPD in the same manner as pointed out above. Moreover, recently, it is reported that PPD is also dependent on the surface orientation of Si substrate such as (110) and (111). Since, in manufacturing of finFETs, various surfaces are exposed to plasma, one should also pay attention to the geometrical effects in designing PPD\cite{49}. In reliability characterization such as NBTI and Hot-Carrier (HC) tests for finFETs, $\Delta V_{th}$ and $I_{on}$ variation may be affected by PPD and PCD. Note that analytical expressions for some mechanisms were reported\cite{30,41,50}, thus, using these frameworks, one can perform variability predictions with lower simulation costs. Therefore, variability enhancement attributed to PPD should be implemented in designing a VLSI circuit with finFETs.

Finally, we pay attention to PCD on high-k dielectrics. Fig. 9a shows obtained charge-to-breakdown under CCS ($Q_{CCS}$) for MOS capacitors.

![Fig. 7](image-url)

**Fig. 7.** (a) Calculated $\Delta V_{th}$ distribution for various $|E_{PCD}|$. (b) Calculated standard deviation of $\Delta V_{th}$ as a function of $E_{PCD}$ for various power-law constants $\eta$.

![Fig. 8](image-url)

**Fig. 8.** Illustrations of PPD creation in a fin structure. As seen on the left, due to the lateral straggling and bombardment of sputtered species, the sidewall surface of the fin is damaged. On the right, MD simulation results after Br impacts ($E_{ion} = 200$ eV, 1000 impacts) are shown. As seen, in addition to the damaged layer near the reaction surface, defects are seen in the fin.

![Fig. 9](image-url)

**Fig. 9.** (a) CCS charge-to-breakdown ($Q_{CCS}$) as a function of stress current density. (b) CVS time-to-breakdown ($t_{CVS}$) as a function of applied electric field. The inset shows cumulative plots of $t_{CVS}$.

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Please cite this article as: K. Eriguchi, K. Ono, Impacts of plasma process-induced damage on MOSFET parameter variability and reliability, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.07.004
damaged by CCP exposure. As seen, $Q_{CCS}$ decreases with plasma exposure time, which is consistent with $\Delta V_{th}$ in Fig. 4a. Fig. 9b, then, shows obtained time-to-breakdown under CVS ($t_{CVS}$) for various applied electric field. In the case of 90-s plasma exposure, both $Q_{CCS}$ and $t_{CVS}$ decrease by plasma exposure (see “Control”). However, in the case of 30-s plasma exposure, $t_{CVS}$ increases in the case of the lowest electric field, in other words, $t_{CVS}$ does not decrease in accordance with the amount of PCD. Based on the results for other PCD measures such as Random Telegraph Noise (RTN) [51] (not shown here), $\Delta V_{th}$, and CCS-TDDB, one confirms that the 30-s plasma exposure inherently degrades MOSFET performance. We have also found that an increase in the junction leakage by the 30-s plasma exposure [52]. It was reported [21] that the direction of $\Delta V_{th}$ in a high-k MOSFET depends on the amount of PCD. The number of generated defects and the distribution of charge trapping sites determine this charging polarity. Since the physical thickness of high-k/IL in this case is ~8.0 nm, the charge trapping effects become more dominant, and, furthermore, high-k dielectrics are naturally sensitive to charge trapping. Owing to the effects of trapped charges, during CVS tests, stress current density $J_{CVS}$ for damaged device was found to become smaller than that for Control. Thus, this mechanism decreases the defect generation rate during CVS tests until the final dielectric breakdown, even if the applied electric field is same. Notice that this finding is considered as another evidence of TDDDB conflicting results [53] in addition to previous data found for an 8-nm-thick SiO$_2$ with various PCD [54] and a 2-nm-thick SiO$_2$ with different mechanical strain [55].

Employing a defect generation model, previous studies proposed a correlation between CCS- and CVS-TDDB data as [53–55]

$$J_{CVS}(t) = \frac{Q_{CCS}(t)}{\int_{0}^{t} Q_{CCS}(\tau) d\tau}$$

where $Q_{CCS}(t)$ is the charge-to-breakdown under CCS with stress current $J$ [55]. Note that in the CVS test, $J_{CVS}$ depends on stress time due to trapped charges, thus, $Q_{CCS}(J_{CVS})$ is generally not constant. This model is based on the so-called cumulative damage law [56] and derived from a simple defect generation model [54]. Since $J_{CVS}$ during the CVS-TDDB test decreases due to the presence of trapped charges or fast trapping sites additionally created by PCD, the decrease in $J_{CVS}$ extends $t_{CVS}$ of plasma-damaged MOS capacitors for some cases in this study. (Note that this effect is valid only for a certain amount of PCD.) Therefore, it is concluded that CVS-TDDB is not versatile for evaluating plasma-induced charging damage in bulk and SOI technologies, Proc. Int. Symp. Plasma Process-Induced Damage 2000, pp. 30–33.

4 Conclusions

We presented comprehensive variability enhancement models for PCD. Ion bombardment creates defects and forms a recess structure, which leads to $\Delta V_{th}$ and a drain current decrease. The parameter variability by plasma fluctuation is predicted by TCAD and a Monte Carlo method. We performed a model prediction of variability enhancement of $\Delta V_{th}$ by the antenna effect using an antenna ratio distribution reported in literatures. Significant enhancement of these parameters is confirmed, implying that one should take into account the intrinsic PID nature in designing and addressing VLSI circuit reliability. It is suggested that modern finFETs are sensitive to PPD and high-k CVS-TDDB methodology should be optimized in the presence of PCD.

Acknowledgments

We greatly thank Dr. Y. Nakakubo and Mr. M. Kamei for their support in damage characterization. This work was financially supported in part by a Grant-in-Aid for Scientific Research 25630293 from the Japan Society for the Promotion of Science.

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