Reliability of high-speed SiGe:C HBT under electrical stress close to the SOA limit

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The reliability of high-speed SiGe:C HBT under electrical stress close to the Safe Operating Area (SOA) limit is analyzed and modeled. A long time stress test, up to 1000 h, is performed at bias conditions chosen according to applications targeted for these transistors. During the aging tests, Gummel plots are measured at fixed time to analyze the evolution of base and collector current. At low level injection, we observed an increase of the base current whereas the collector current remains constant for the whole Vbe range and during the 1000 h aging time. By means of 2D TCAD simulations, this evolution of base current is attributed to trap activity at the emitter-base junction periphery. Based on TCAD simulation results, we propose an aging law using a differential equation that has been implemented in HiCUM L2 v2.33. This reliability-aware compact model allows designers creating reliability-aware circuit architectures at an early stage of the design procedure, well before real circuits are actually fabricated.

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1. Introduction

In the on-going evolution toward millimeter-wave circuits, silicon-germanium (SiGe) heterojunction bipolar transistors (HBT) prove their competitiveness against Si CMOS and III–V semiconductor technology. Unfortunately, the cost of this evolution is a decrease of the collector-base and open base collector–emitter breakdown voltages (BVCE0 and BVCE, respectively), which are measured as 5.2 V and 1.5 V for the technology investigated in this paper, limiting the Safe Operating Area (SOA).

To analyze this impact, aging tests have been performed under electrical stress close to the SOA limit. After the stress test campaign, using Sentaurus TCAD device simulations, the physical background of the degradation is explained and an aging law is extracted and implemented in HiCUM L2 v2.33 model [2].

2. Technology and experimental procedure

Measurements and aging tests were performed on SiGe:C NPN HBT manufactured by Infineon Technologies AG [3]. HBTs feature a peak cut-off and oscillation frequency of 240/380 GHz, respectively. A double collector configuration (CBEBC) is used, with a single drawn emitter size of $0.2 \times 10 \, \mu m^2$. Test structures have a GSG-configuration with emitter and substrate connected to the ground pad. As required for long-time stress tests (i.e. 1000 h), stress tests and measurements were realized using encapsulated devices. The samples were biased in a common-emitter configuration at constant and controlled ambient temperature of 300 K. To characterize the evolution of the base and collector currents during aging test, a Gummel plot at Vbc = 0 V is performed at fixed time of 1 h, 3 h, 7 h, 24 h, 36 h, 48 h, 72 h, 120 h, 250 h, 500 h, 750 h and 1000 h. Moreover, at 300 h, an additional point is added with 24 h between the end of the stress test and the measurement. Three bias conditions, P1, P2 and P3, according to SOA, are used during 1000 h, as highlighted in Fig. 1. The first bias condition P1 is defined below the BVCE0, at 1 V for collector voltage and at high collector current density, fixed at 10 mA/μm2. The second bias points, namely P2 and P3, are defined above BVCE0 with a collector voltage fixed at Vce = 2 V and Vce = 3 V, respectively, and a collector current density fixed at Jc = 5 mA/μm2 and Jc = 1 mA/μm2, respectively.

3. Aging test results

The tests are performed on 6 HBTs for each bias condition, hence 18 HBTs under test in all. The base current function of Vbc have been measured (at Vbe = 0 V) during the aging tests. Regardless of the stress conditions, the DC characteristics of the base-collector junction are not significantly affected by the aging test. Considering the base-emitter...
junction, Fig. 2 shows the base and collector current as a function of Vbe (Vbe = 0 V) during the aging test under P1 (a), P2 (b) and P3 (c) conditions.

- At P3 bias stress, the base current increases regularly with stress time at low Vbe. At Vbe = 0.65 V, the variation is 120 nA after 1000 h of aging (Fig. 3c).
- At P2 bias stress, the base current slightly increases for low Vbe. At Vbe = 0.65 V, the variation after 1000 h is 80 nA (Fig. 3b).
- At P1 condition, the DC characteristics show no significant increase (Fig. 3a).

Briefly, the higher Vce is, the more the low-injection level base current increases with the aging time. This evolution could be attributed to impact ionization occurring within the base-collector space charge region and creating hot carriers. Subsequently, the hot carriers create increasing trap density at the emitter-base spacer edge [4,5]. The activity of those traps is associated with increasing generation-recombination currents. Note that a natural slight recovery is observed if the device stay “on the shelf” between two aging periods. This recovery is visible at 300 h in Fig. 3.

4. TCAD Simulation

To get deeper insight into the physical origin of base current variations, a half structure of the HBTs is simulated with Sentaurus TCAD. The simulations are performed using calibrated hydrodynamic model and calibrated transport parameters for SiGe HBTs [6,7].

4.1. Calibration before aging

To fit the base current measurement in the 0.7 V–0.9 V Vbe range, Auger model [8] is activated and the coefficient A of Eq. (1) is reasonably set to 1.2 \times 10^{-29} \text{cm}^3 \text{s}^{-1} \text{cm}^{-2} for electrons and holes, respectively.

\[
C_n(T) = \left( A_{n,n} + B_{A,n} \left( \frac{T}{T_0} \right) + C_{A,n} \left( \frac{T}{T_0} \right)^2 \right) \left[ 1 + H_n \exp \left( \frac{E_n}{N_{0,n}} \right) \right]
\]  \hspace{1cm} (1)

To fit the base current at Vbe lower than 0.7 V, SRH recombination is used. After several tests, the SRH recombination with high-field enhancement and doping dependence is activated. The Nref parameter of doping dependence Eq. (2) is set to 1.0 \times 10^{13} \text{cm}^{-3}.

\[
\tau_{dop}(N_{A,0} + N_{D,0}) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left( \frac{N_{A,0} + N_{D,0}}{N_{ref}} \right)}
\]  \hspace{1cm} (2)

A good agreement between the TCAD model and measurement can be observed (see Fig. 4). Moreover, when packaged devices are considered (for the aging tests purpose), leakage currents occur at base and collector terminals. This effect can be simulated by adding compact resistors between transistor terminals, R_{BE}, R_{BC} and R_{CE} (close to 200 M\Omega each), and performing mixed-mode simulation of the complete circuit [9], including the 2D HBT and lumped resistors (see red triangles in Fig. 4).

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4.2. Analysis of aging devices

For the stressed devices, calibrated models described in 4.1 are kept. Since electrical characteristics of devices aged at P1 stress condition remain almost constant during the aging test, only P2 and P3 bias conditions are considered in this part.

Due to the collector voltage above $BV_{CEO}$ for P2 and P3, electron-hole pairs are created in the base-collector space charge region by impact ionization. These hot carriers become enough energetic to break the dangling bond at the emitter-base spacer [4,5]. Therefore, the base current evolution is modeled by adding trap density at the interface between extrinsic emitter-base junction and emitter-base spacer. At each stress time, a uniform acceptor type trap density is defined at a fixed level $E_T$ placed at $E_T - E_V = 0.6$ eV, being $E_V$ the valence band energy level.

For each stress time, a value of the trap density $N_T$ was extracted. Fig. 5 presents the extracted values of the trap density at base-emitter junction as a function of time for HBT aged at P3 and P2 conditions. For P3 and P2 conditions, the trap density increased drastically during the first aging hours; afterward, the trap density stabilizes to reach a saturation value. However, trap density saturation value for P3 is higher than for P2. This higher trap density is due to a more important impact ionization effect due to the higher collector voltage in the case of P3 compared with P2.

As in [10] and [11], an exponential Eq. (3) is used to describe the evolution of the trap density in function of the aging time.

$$N_T(t) = N_T\text{final} \left(1 - \frac{N_T\text{initial}}{N_T\text{final}} \right) \exp \left(\frac{-t}{\tau}\right) \tag{3}$$

Equation parameters were extracted; with $N_T\text{final}$, $N_T\text{initial}$ and $\tau$ equal to $1.6 \times 10^{12}$ cm$^{-2}$, $6.6 \times 10^{11}$ cm$^{-2}$, and 65 h for P2 and $2.5 \times 10^{12}$ cm$^{-2}$, $1 \times 10^{12}$ cm$^{-2}$, 70 h for P3, respectively, results depicted in Fig. 5 were obtained. The time constant $\tau$ is roughly the same for both bias conditions, while for P3 the parameters $N_T\text{final}$ and $N_T\text{initial}$ are higher than for P2.
5. Compact modeling

5.1. Aging law

The evolutions of electrical characteristics during aging test are attributed to trap activity at the emitter-base junction periphery. In HiCuM model [2], the base current in this region is modeled by:

\[ i_{BEP} = I_{BEP0} \exp \left( \frac{v_{BE}}{m_{REP} V_T} \right) - 1 + I_{REP} \left[ \exp \left( \frac{v_{BE}}{m_{REP} V_T} \right) - 1 \right] \]  

(4)

where the saturation currents \( I_{BEP0} \) and \( I_{REP} \) as well as the non-ideality factors \( m_{REP} \) and \( m_{REP} \) are model parameters.

The parameters \( I_{BEP0} \) and \( m_{REP} \) are extracted at initial time and kept constant during aging test while recombination parameters, \( I_{REP} \) and \( m_{REP} \), are extracted from the measurement at the different stress times. The parameter mainly responsive for the base current increase is \( I_{REP} \), while \( m_{REP} \) remains almost constant.

According to [10], the evolution of the parameter \( I_{REP} \) is proportional to the trap density evolution. The Eq. (5), based on Eq. (3), is used to describe the \( I_{REP} \) evolution as a function of the aging time.

\[ I_{REP} = I_{REP0} \left[ \exp \left( \frac{t}{\tau} \right) - 1 \right] \]  

(5)

To implement this aging law in Verilog A, a differential Eq. (6) is used. Eq. (5) is the solution of the Eq. (6) with the generation rate of trap \( G = I_{REP0}/\tau \) and the probability of traps annihilation \( R = 1/\tau \).

\[ \frac{dI_{REP}}{dt} = G - R \cdot I_{REP} \]  

(6)

A value of \( 2.57 \times 10^{-2} \text{ A s}^{-1} \) for P2 and \( 6.66 \times 10^{-20} \text{ A s}^{-1} \) for P3 is extracted for G and R, respectively. The recombination rate \( R \) is the same for P2 and P3, while the generation rate \( G \) increases with Vcb.

5.2. Implementation in HiCuM model

In order to include the aging law in HiCuM model, we need to implement three additional parameters, namely \( G, R \) and \( \text{ATSF} \).

- The \( G \) parameter is proportional to the impact ionization effect, occurring at high collector voltage. The impact ionization effect is modeled in HiCuM by the avalanche current, \( I_{avl} \) [12]. Eq. (7) defines the generation rate \( G \), according to bias conditions

\[ G(I_{avl}) = A \cdot I_{avl} + G_0 \]  

with \( A = 7.575 \times 10^{-21} \text{ s}^{-1} \) and \( G_0 = 0.75 \times 10^{-8} \text{ A s}^{-1} \).

- The recombination rate \( R \) parameter is a constant, fixed at \( 3.7 \times 10^{-8} \text{ s}^{-1} \).

- A value of \( 2.57 \times 10^{-2} \text{ A s}^{-1} \) for P2 and \( 6.66 \times 10^{-20} \text{ A s}^{-1} \) for P3 is extracted for G and R, respectively. The recombination rate \( R \) is the same for P2 and P3, while the generation rate \( G \) increases with Vcb.

6. Conclusion

We present the result of long time aging test performed at bias condition close to the SiGe HBT SOA limit. The increase of the low injection base current is quantified for a range of bias conditions that is important for applications.

According to TCAD simulation, the degradation of the base current is the result of traps activity generated by hot carriers’ damage in the emitter–base junction periphery.

Based on these 2D simulation results, an aging law is extracted. A differential equation for theVerilog A implementation in HiCuM model has been proposed and simulation results are compared to measurement. A good agreement is obtained between measurements and simulations as function of the aging time.

As explained in [13], this reliability-aware compact model should allow designers creating reliability-aware circuit architectures at an early stage of the design procedure, well before real circuits are fabricated.
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