Experimental investigation on the evolution of a conducted-EMI buck converter after thermal aging tests of the MOSFET

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ABSTRACT

The electrical characteristics of semiconductors and especially the power components are sensitive to temperature variation. Therefore, the thermal behaviour takes an essential place in the design phase. This phase can predict the reliability of semiconductors, its lifetime and the evolution of its performances versus time. Recent studies have been interested in electromagnetic interferences (EMI) variation and in the accelerated aging tests of the power components' effect on their static and dynamic characteristics. This paper presents an experimental investigation of the thermal aging effect of power MOSFETs on the EMI evolution generated by a buck converter circuit. Thermal aging tests are applied on the N-MOS transistors in normal operating conditions in a chopper circuit with a load current of 250 mA. This is in order to promote the thermal effect compared to the electrical one. The impressive thermal aging effect on the amplitude of the conducted EMI, on the switching time, has been discussed.

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1. Introduction

The recent tendency to the miniaturization of components and the use of embedded electronics in systems with high thermal stress makes the thermal aspects to be taken into account at the level of both conception and exploitation [1,2]. The power transistors MOSFET are more and more used in new technologies, especially in the fields of transportation (aeronautics, railway and automobile) and energy conversion.

The reliability study of the power components plays an essential role in designing of current systems [3–5].

2. Aging technique and measurement process

2.1. Aging technique

As part of its applications, the MOSFET incurs important variations in junction temperature. The latter often causes the failure of these power components.

The estimate of the MOSFET lifetime, during its normal operation, encourages us to put it under severe stress (thermal aging tests). The MOSFET under test is placed in a power application (DC/DC buck converter) as presented in Fig. 1.

The switching cell is constituted of a MOSFET transistor, a freewheeling diode and a resistor (R) and an inductor (L) for the load. It is supplied with a voltage source of 30 V following a current of 250 mA to the load, at a 50 kHz switching frequency with a duty cycle of 50%. To reduce the influential parameters on the results, we have used for the

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freewheeling diode a second transistor (MOSFET_1) similar to the one used for the switching (MOSFET_2). For the transistor (MOSFET_1), a short-circuit is made between the gate and the source to use the transistor body diode as a freewheeling diode. The switching cell can represent an inverter leg because it is constituted of two MOSFET transistors.

Our methodology consists in putting the transistor (MOSFET_2) under test in a heating system where we maintain a temperature of 170 °C. The load consumes a current limited to 250 mA in order to promote the thermal aging effect compared to the electrical aging effect.

2.2. Measurement process

Our measurement process consists in inserting an EMC filter called Line Impedance Stabilization Network (LISN), between the power supply and the DC/DC converter. The LISN allows canalising the Conducted Electromagnetic Interferences (CEMI) to be measured [6]. Fig. 2 shows how the LISN has been inserted.

The EMC standard [9] sets the LISN type to use for the CEMI. The victim is normally outside the converter, so it is either inside the supply network and/or the load. Nevertheless, the LISN canalizes the CEMI to its 50 Ω impedance.

The CEMI voltages are calculated using Eq. (1) for the differential mode (V_{DM}) and Eq. (2) for the common mode (V_{CM}):

\[ V_{DM} = V_{R1} - V_{R2} \]
\[ V_{CM} = \frac{V_{R1} + V_{R2}}{2} \]

where \( V_{R1} \) and \( V_{R2} \) are the voltage measured in the external resistances \( R1 \) and \( R2 \) of the LISN.

Thereafter, we compare the common mode and the differential mode spectra before and after different aging periods. The measurement process is shown in Fig. 3.

To obtain credible results, we have repeated the same aging test on many MOSFETs. Thus, we have used 10 samples of the IRF730 transistors, which are characterized according to their datasheet by:

- a maximum \( V_{th} \) voltage = 400 V.
- A maximum \( I_{th} \) current = 5.5 A at 25 °C.
3. Results and discussion

3.1. Aging effect on the conducted EMI spectra

A simple Fast Fourier Transformation (FFT) calculation of $V_{CM}$ and $V_{DM}$ allows us to deduce the EMI versus frequency (spectrum).

We will study in this part the accelerated thermal aging effect on the common and differential mode spectra. Figs. 4 and 5 show the variation in the amplitudes of the two modes before and after aging tests.

Hereafter, we propose to study the aging effect on the amplitude disturbance around a specific frequency. Precisely, we choose the frequency of 9.7 MHz.

Table 1 shows the amplitude variation of both voltages: common and differential mode voltages.

In Fig. 6, we have drawn the evolution of the common mode interference variation $\Delta V_{CM}$ versus aging time.

The $\Delta V_{CM}$ variation evolves in a nonlinear manner according to the aging time. We notice that after 150 min, $\Delta V_{CM}$ is almost constant.

3.2. Aging effect on the $V_{th}$ evolution

Recent literatures have demonstrated that after a thermal aging application on the MOSFETs, the threshold voltage $V_{th}$ increases [10–12].

According to [15] the value of the gate-drain capacitance $C_{gd}$ decreases in a low manner after thermal aging. In previous research works [13, 14] we showed that an increase in the $V_{th}$ and a decrease in the $C_{gd}$ caused an increase in the amplitude of the CEMI. This confirms the measurement results presented before in this paper, which show a notable increase of the CEMI after accelerated thermal aging of the MOSFET.

![Fig. 6. Common mode variation $\Delta V_{CM}$ in terms of aging time (components 1, 2 and 3).](image1)

Table 1:

<table>
<thead>
<tr>
<th>Aging time (min)</th>
<th>CM (dBμV)</th>
<th>$\Delta V$ (dBμV)</th>
<th>DM (dBμV)</th>
<th>$\Delta V$ (dBμV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>27.85</td>
<td>0</td>
<td>44.50</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>30.36</td>
<td>2.51</td>
<td>44.90</td>
<td>0.4</td>
</tr>
<tr>
<td>60</td>
<td>33.8</td>
<td>5.95</td>
<td>45.22</td>
<td>0.72</td>
</tr>
<tr>
<td>90</td>
<td>36.6</td>
<td>8.75</td>
<td>40</td>
<td>−4.5</td>
</tr>
<tr>
<td>120</td>
<td>40.8</td>
<td>12.95</td>
<td>46.37</td>
<td>1.87</td>
</tr>
<tr>
<td>150</td>
<td>44.06</td>
<td>16.21</td>
<td>47.68</td>
<td>3.18</td>
</tr>
<tr>
<td>180</td>
<td>44.08</td>
<td>16.23</td>
<td>47.63</td>
<td>3.13</td>
</tr>
<tr>
<td>210</td>
<td>44.13</td>
<td>16.28</td>
<td>48.41</td>
<td>3.91</td>
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</tbody>
</table>

![Fig. 7. Threshold voltage evolution according to the aging time (components 7 and 8).](image2)

Table 2:

<table>
<thead>
<tr>
<th>Aging time (min)</th>
<th>$V_{th}$ (V)</th>
<th>$\Delta V_{th}$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Component 7</td>
<td>Component 8</td>
</tr>
<tr>
<td>0</td>
<td>3.32</td>
<td>3.24</td>
</tr>
<tr>
<td>30</td>
<td>3.48</td>
<td>3.28</td>
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<tr>
<td>120</td>
<td>3.74</td>
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<tr>
<td>150</td>
<td>3.79</td>
<td>3.41</td>
</tr>
<tr>
<td>180</td>
<td>3.85</td>
<td>3.50</td>
</tr>
</tbody>
</table>

Among the aging criteria used in our study is the variation of 100 mV of the threshold voltage $V_{th}$.

Table 2 presents the evolution of $V_{th}$ with respect to the stress time for two components at 170 °C.

Fig. 7 presents the evolution of the threshold voltage $V_{th}$ during 250 min of the aging test.

The $\Delta V_{th}$ values plotted here correspond to the $V_{th}$ evolution, compared to the initial value. Based on these data, we demonstrate that after a thermal aging application on the MOSFET, the threshold voltage $V_{th}$ increases.

3.3. Aging effect on the switching time evolution

In this part, we discuss the thermal aging effect on the switching signal parameters, such as the rise time and the fall time.

Figs. 8 and 9 illustrate respectively the MOSFET turning off and on for different aging times.

We note from these figures that the $V_{ds}$ voltage incurs a shift to the right by the thermal aging. This shift has revealed that the conduction of the transistor is made with a delay whose value is less than a microsecond. This is explained by the increase in the threshold voltage $V_{th}$ of the MOSFET after aging, as clarified previously and as given in the literature [10–12].

However, we note that there is an inconclusive progress at the MOSFET rise or fall time. This is consistent with the results of the work presented in [16], where the authors argued that the MOSFET rise time incurred a random variation after thermal aging.

Table 3 presents the rise time and fall time evolution according to the aging time.

The analysis of the rise time and fall time of components 9 and 10, shown in the above table, presents that the thermal aging affects them. A random variation at two times is observed.

![Fig. 8. MOSFET turning off for different aging times.](image3)

![Fig. 9. MOSFET turning on for different aging times.](image4)

Table 3:

<table>
<thead>
<tr>
<th>Aging time (min)</th>
<th>Component 9</th>
<th>Component 10</th>
<th>Component 9</th>
<th>Component 10</th>
</tr>
</thead>
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<td>500</td>
<td>500</td>
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<td>150</td>
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</table>

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Secondly we found in the literature a model that express the evolution of $V_{th}$ variation according to the aging time ($\Delta V_{th} = A \times t^n$) and that this model inspired us to propose a similar model for conducted EMI evolution according to the aging time. We present also a progress of the rise time and fall time of MOSFET after aging. The result of measurements presented in Table 3 summarizes the evolution of both rise time and fall time after thermal aging. We show that these times have undergone a random variation. And this is consistent with the results of the work presented in [16], where the authors argued that the rise time of MOSFET underwent random variation after heat aging. According to this significant impact, we conclude that the thermal aging is an important factor affecting the conducted EMI amplitude. Therefore, we can use the conducted EMI variation, such as the signature of the aging MOSFET.

5. Conclusion

This paper presents an experimental investigation of the electrical and electromagnetic performances of a MOSFET after thermal aging tests. A thermal aging test bench has been performed under conditions similar to those of a real operation. After various accelerated aging periods, we see a significant increase in the conducted EMI amplitude. The monitoring of the conducted EMI evolution over time allows us to determine when to intervene in the system using these components to prevent a potential failure due to a problem of immunity of certain other sensitive system components and this because of the increased electromagnetic interference.

The study presented in this paper is made on a power conversion application used in the automotive field.

Finally, a model of the conducted EMI evolution based on the accelerated aging time will be the focus of our future research.

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