Improvement of MOSFET matching characterization with calibrated multiplexed test structure

L. Welter \textsuperscript{a,b,*}, J.L. Scotto di Quaquero \textsuperscript{a}, P. Dreux \textsuperscript{a}, L. Lopez \textsuperscript{a}, H. Aziza \textsuperscript{b}, J.M. Portal \textsuperscript{b}

\textsuperscript{a} STMicroelectronics, Rousset, France
\textsuperscript{b} Aix Marseille Université, CNRS, IM2NP UMR 7334, Marseille, France

A R T I C L E   I N F O

Article history:
Received 25 May 2015
Received in revised form 24 June 2015
Accepted 24 June 2015
Available online xxxx

Keywords:
MOSFET matching
Test structure
Multiplexing

A B S T R A C T

This paper presents a way to implement a test structure able to measure accurately a large number of threshold voltage values for Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) matching characterization. A multiplexed system able to select a single transistor among others in a small array is used. This architecture guarantees a similar environment for all transistors in the array, while requiring a small number of pads for measurement. Moreover, the influence of the multiplexer switches can be evaluated: their unwanted contribution to the measurement can therefore be compensated. An experimental study to evaluate the influence of this multiplexer on measurement and the efficiency of the compensation is conducted. Silicon results are presented in order to validate the concept.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

Improvement of the semiconductor manufacturing process over the last decades has allowed to decrease size and power consumption of chips and to increase their functionalities in the same time. However, this improvement tends to increase the process complexity, leading to the need of monitoring a rising number of critical parameters in order to keep a good yield.

Among these parameters, there is the threshold voltage ($V_T$) of MOSFETs that may undergo local variations called mismatch. These variations mainly cause issues in analog parts of Complementary Metal–Oxide–Semiconductor (CMOS) circuits \cite{1} as well as in Static Random Access Memories (SRAMs). For matching evaluation, a statistically significant number of threshold voltage differences ($\Delta V_T$) is needed in order to calculate a standard deviation ($\sigma \Delta V_T$). This allows extracting the threshold voltage matching parameter ($A_{VT}$) which depends on the transistor channel length ($L$) and width ($W$), as presented in Eq. (1).

$$\sigma \Delta V_T = \frac{A_{VT}}{\sqrt{W \times L}} \tag{1}$$

Throttle voltages are commonly monitored on dedicated test structures located on silicon wafers between the chips in the scribe lines as shown in Fig. 1. These structures are tested with probe cards and have a limited number of pads. That is why, measuring independently a large number of transistors within a single test structure is impossible without using a multiplexed system. Indeed, a multiplexed system allows several transistors in an array to share the same pads and can be selected one after another.

Techniques using multiplexers already exist for $\Delta V_T$ local variation measurement \cite{2–5}. The main drawback of these structures is related to the array size. Indeed, such large structures can be prone to process gradient \cite{6} that can influence the measurement.

Large structures also cause problems regarding transistor’s environment: transistors inside or at the suburbs of the array do not have the same wiring nor the same distance to bulk connection. The other drawback is the multiplexed system itself that can induce variability \cite{7}. Furthermore, some structures are even too large to be placed in scribe lines \cite{8}.

This paper proposes an alternative solution to these limitations. First, array size is reduced to solve the transistors’ environment issue but also to allow the whole structure to fit into regular scribe lines. This permits the evaluation of transistors matching on a whole wafer with standard parametric test measurement instruments, in a production context. Besides, the influence of the array multiplexers can be evaluated and thus compensated to ensure an optimal accuracy.

The rest of the paper is organized as follows: the second section focuses on the multiplexed test structure presentation. Section 3 exposes a complete simulation analysis of the structure, with an evaluation of the multiplexed system influence. Section 4 presents silicon data. Finally, Section 5 gives some concluding remarks.
2. Multiplexed test structure

2.1. Presentation of the structure

The presented structure is composed of small $2 \times 2$ elementary arrays of transistors. This arrangement allows to measure up to 6 $\Delta V_T$ within a single array as shown in Fig. 2. Each array shares the same drain pad through a switching system. The arrays are grouped 2 by 2, and the formed groups also share a common source pad. All the groups present on one structure have a common bulk and a common gate pad, as presented in Fig. 3.

2.2. Switches description

The switches have 3 positions as shown in Fig. 3: open, closed in position 1 (drain pad is connected to a transistor), and closed in position 2 (drain pad is directly connected to the shared source pad of the group). When the switch is in position 1, the system is in measurement mode. When the switch is in position 2, the system is in evaluation mode. In this case the transistor is bypassed and the influence of the switch can be evaluated.

These 2-positions switches are made of 2 NMOS and 2 PMOS transistors, arranged in pass-gate. These 2 pass-gates are controlled by 2 signals: $\text{eval}$ and $\text{measure}$, as shown in Fig. 4. These signals control directly the NMOS transistors and are inverted to control the PMOS transistors.

2.3. Switches control system

A shift register [9] coupled with some 1 to 2 decoder generates the $\text{eval}$ and the $\text{measure}$ signals as presented in Fig. 5. The working principle is based on the use of the shift register to select the switch to control. The decoder is used to set the selected switch in measurement or in evaluation mode. If a switch is not selected by the shift register, it remains open. This solution requires only 3 pads to work and can control an unlimited number of switches.

3. Simulation of the mismatch impact over the switches

3.1. Measurement principle

There are many ways to measure the $V_T$ of a transistor [10]. The method used here is the constant current method. Simulation results are given for a CMOS 90 nm technology with a 1.2 V nominal voltage for transistors and a nominal gate oxide thickness of 21 Å.

To extract the $V_T$, a 25 mV is applied between drain and source nodes ($V_{DS}$), and the gate voltage node ($V_G$) is tuned until the drain current $I_D$
Fig. 4. Schematic of the array's switches.

Fig. 5. Schematic of the control system.

Fig. 6. Switches influence when the first transistor of an NMOS array is measured.
reaches an arbitrary fixed value depending on the size of the transistor, as presented in Eq. (2). For the extraction, a drain current of 40 nA is chosen as the standard fixed value for the given technology.

\[ I_D = 40 \times 10^{-9} \times \frac{W}{L} \text{ when } V_G = V_T \]  

(2)

Reference \( \sigma \Delta V_T \) have been extracted for various transistors sizes with this method.

### 3.2. Influence of switches on \( V_T \) measurement

The switches composing the multiplexed system are made with large transistors. Consequently in measurement mode, open switches can be schematized as large resistors \( (R_{OFF}) \) whereas closed switches have a negligible resistance, but leaks through their gate oxide.

The pass-gate transistor mainly affected by gate leakage is the transistor that transmits the signal. For example, while measuring an NMOS transistor, the drain voltage is 25 mV and so the NMOS of the pass-gate transmits the signal as shown in Fig. 6.

The gate leakage in this case is around 1 nA, so if a current of 40 nA is measured on the drain pad, the current that flows through the measured transistor is actually 41 nA. This gate leakage can induce a shift of up to 800 µV on the \( V_T \) of the measured transistor.

### 3.3. Influence of switches mismatch on \( V_T \) measurement

Basically, what really matters is not the absolute value of the current flowing through the measured transistor. Indeed, mismatch evaluation is based on threshold voltage differences, so if all switches leak similarly, it is not an issue.

In fact, switches are also mismatched, and it is important to evaluate the influence of their mismatch on the transistor \( V_T \) measurement. For simulation purpose, measured transistors are perfectly matched and previously characterized for this technology.

In these conditions, 240 Monte-Carlo simulations with local variation on typical process setup have been performed. These local variations alter the \( V_T \) and the gain (\( \beta \)) of BSIM4 model transistors. The variation domain of these parameters is defined according to parameters previously characterized for this technology.

Results presented in Table 1 show that a mismatch between the switches can lead to an error of up to 1.5% on the final calculated \( \sigma \Delta V_T \). This error comes mainly from the variation of the gate leakage current of the pass-gate transmitting transistor \( (I_{\text{GATE LEAK}}) \) as shown in Fig. 8.

### 3.4. Switches influence compensation

In order to compensate the variation of this leakage, the switches are set in evaluation mode as shown in Fig. 9.

In this case, the current is mainly flowing directly from the drain pad to the source pad of the array. The measuring principle is to force a 40 nA current on the source pad to virtually replace the measured transistor, and then to measure the current flowing through the drain. By subtracting the measured current with the current forced on the source pad, it is possible to know the gate leakage. Indeed \( V_{DS} \) is reduced to approximately 10 µV in this mode: \( I_{\text{OPEN}} \) is thus negligible.

Now if the measurement is performed with the new calculated current, the error on calculated \( \sigma \Delta V_T \) is reduced to at most 0.11% as shown in Table 2. This makes the multiplexing solution a good choice for mismatch evaluation.

### 4. Silicon measurement results

#### 4.1. Layout concerns

The multiplexer is implemented on a 22-pads test structure. Such a structure embeds 5 groups of 8 transistors – so 40 transistors grouped in 10 arrays – allowing to measure up to 60 \( \Delta V_T \).

The 4 transistors composing a switch are layouted 2 by 2 with the common-centroid method to ensure that they have the similar influence in both evaluation and measurement mode. The wiring and the layout of the 4 transistors and their associated control system are entirely symmetrical in order to have the same influence on measurement. An array including the switches that fits between 2 test pads is presented in Fig. 10. The final structure with its 5 groups of transistors has the same dimension as a standard test structure (i.e., 3000 × 80 µm).

#### 4.2. Measurement results

Measurements have been performed on 3 different transistors dimensions for NMOS and PMOS. 10 × 10 and 1 × 1 sizes have been measured with the multiplexed system. 3.1 × 1 size is characterized with pairs of MOS, in a classical way without multiplexer.

Silicon results show a good correlation with theoretical \( A_{VT} \) previously calculated as shown in the Pelgrom’s plots [11] in Fig. 11. Moreover, the 3 aligned points shows that the switches do not induce a significant shift compared to standard measurement method without multiplexing.

![Fig. 7. Monte-Carlo Simulation conditions.](http://dx.doi.org/10.1016/j.microrel.2015.06.104)

![Fig. 8. Current due to switches mismatch while measuring a 10 × 10 NMOS transistor.](http://dx.doi.org/10.1016/j.microrel.2015.06.104)

---

Please cite this article as: L. Welter, et al., Improvement of MOSFET matching characterization with calibrated multiplexed test structure, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.06.104
5. Conclusion

A method using calibrated multiplexers to measure a statistically significant amount of $V_T$ over one single standard-size test structure is presented in this paper. The measurement accuracy and the test structure functionality have been validated through silicon results. The usage prospects are interesting in a production context since such structure allows performing transistor matching results mappings over a whole wafer at parametric test step level.

In addition, being able to measure 40 transistors without moving the probe card could also reduce test time. Therefore, this method might also be extended to other electrical parameters to characterize different devices on wafers.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$\sigma \Delta V_T$ (µV)</th>
<th>% of ref. $\sigma \Delta V_T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 x 1 NMOS</td>
<td>0.92</td>
<td>0.01%</td>
</tr>
<tr>
<td>10 x 10 NMOS</td>
<td>0.93</td>
<td>0.11%</td>
</tr>
<tr>
<td>1 x 1 PMOS</td>
<td>0.71</td>
<td>0.01%</td>
</tr>
<tr>
<td>10 x 10 PMOS</td>
<td>0.66</td>
<td>0.10%</td>
</tr>
</tbody>
</table>

References


Please cite this article as: L. Welter, et al., Improvement of MOSFET matching characterization with calibrated multiplexed test structure, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.06.104


